ULTRA LOW POWER AND INTERFERENCE ROBUST TRANSCEIVER TECHNIQUES FOR WIRELESS SENSOR NETWORKS

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by

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I would like to dedicate this thesis to my parents
Abstract

Wireless sensor networks (WSNs) have the potential to build breakthrough technologies for a variety of applications to improve human life. Some of the important applications are prevention, prediction and rescue of disasters, medical study and cure, improve the energy efficiency of homes and industries and study environments in remote places. These applications desire an ultra low power sensor node to extend the battery life, so that minimum or zero maintenance is required after initial installation. With the advancement of CMOS technology, power consumption of processors and semiconductor memories has reduced drastically. However, the radio transceiver power consumption has not experienced much power reduction because of its RF analog circuits. This makes the transceiver the bottleneck with respect to lifetime in existing sensor nodes. Another growing challenge for the sensor node transceiver is its interference robustness. Therefore there is a need of ultra low energy and interference robust wireless transceivers to enable WSNs to thrive in several applications which are not yet successful.

This thesis targets an energy optimized and interference-robust radio communication system for WSNs. Special focus is given to the receiver, as the receiver is either always ON or ON for more time than the transmitter for duty-cycled radio and hence it is the critical part of the transceiver performance both in terms of power reduction and interference mitigation. A system level optimization of the transceivers is carried out, and circuit techniques are proposed to reduce the receiver power consumption.

To reduce the energy consumption of a duty cycled wireless sensor network transceiver, an optimization method is proposed combining fundamental system relations. The method leads to the optimum choice of noise figure and data rate for a given application and transceiver architecture. Considering a set of typical transceiver parameters, it is shown that the energy consumption can indeed be reduced with about 30% or more with this approach compared to the existing approached of choosing either data rate or noise figure. Moreover, this method is also proven to be effective to reduce energy of a transceiver system with a duty-cycled wakeup receiver.
In most transceiver architectures, quadrature generating frequency dividers consume a significant part of the total power. To reduce divider power consumption, still maintaining low output jitter, flipflops for the divider have to be chosen appropriately. An analytic comparison is performed between two types of flipflops, the dynamic transmission gate logic, i.e DTGL and current mode logic i.e. CML. Comparison show that the DTGL flipflop is better for the targeted frequency range in the 90 nm CMOS process, and its benefit increases with reduction of technology feature size.

To improve the interference robustness, a chirped-LO based spread spectrum modulation scheme is proposed for FSK and PSK transceiver systems. Chirped-LO based spread spectrum scheme has a potential of ultra low power consumption with simple receiver architecture compared to other spread spectrum schemes. An analysis of the chirped-LO system show that the bit error ratio (BER) of the chirped-LO systems is better than the corresponding non-chirped system when the interference frequency is close to the carrier frequency. The interference robustness of the chirped-LO system is independent of the interference frequency location. Simulation results confirm this analysis.

A BER analysis of a chirped-LO direct conversion FSK receiver shows that the in-band interference robustness, i.e. the interference to signal ratio (ISR), can be increased by using a higher chirp bandwidth and a low number of data bits in one chirp. A novel 3-phase direct conversion receiver architecture along with a low power demodulator is designed to reduce receiver energy consumption. The proposed receiver, fabricated in 65 nm CMOS technology, is able to achieve a datarate of 8 Mbps and a sensitivity of -70 dBm at BER of $10^{-3}$, consuming only 219 $\mu W$ of continuous power from a 1.2 V power supply operating at a RF frequency of 2.45 GHz. Hence it achieves an energy efficiency of 27 pJ/bit, three times better than the previously reported receivers. In the chirped-LO mode, using a chirp spread bandwidth of 360 MHz, the receiver can achieve a $10^{-3}$ BER at an interference to signal ratio of 8 dB across the whole frequency range with only 15 $\mu W$ of extra power dissipation and a sensitivity degradation of less than 4 dB. This interference robustness is 13.5 dB higher than previously reported interference robustness of ultra low power/energy receivers when the results were published.

The ultra low energy techniques that are proposed and proven here can be incorporated in WSNs radios to significantly improve the battery life time of a sensor node. The interference robustness technique proposed can be used to improve the robustness of a wireless sensor network operating with other communication standards.
Samenvatting

Draadloze sensor netwerken (Wireless Sensor Networks - WSN’s) zijn netwerken van vele kleine autonome sensoren die toegepast kunnen worden op vele gebieden. Enkele van de belangrijkste toepassingen zijn preventie, voorspelling en het bestrijden van rampen; medische studies en applicaties in de gezondheidszorg; het verbeteren van de energie-efficiëntie van woningen en industrie; en omgevings onderzoek op afgelegen plaatsen. Deze toepassingen kenmerken zich allen door de noodzaak van sensor nodes met ultra laag energie verbruik, zodat er minimaal of geen onderhoud nodig is na de eerste installatie (bijvoorbeeld om een batterij te vervangen). Met de verdere ontwikkelingen van CMOS-technologie is het stroomverbruik van processoren en geheugens drastisch verminderd. Echter, het stroomverbruik van de radio-zendontvanger is nog nauwelijks verminderd vanwege de RF (Radio Frequency) analoge elektronica. Dit maakt de radio-zendontvanger het knelpunt in de levensduur van bestaande sensor nodes. Een andere groeiende uitdaging voor sensor nodes is de robuustheid tegen storingen. Daarom is er een behoefte aan ultra lage energie en storingsrobuuste draadloze radio’s om WSN’s in staat te stellen om succesvol te functioneren in allerlei toepassingen en omgevingen.

Dit proefschrift richt zich op een energie-geoptimaliseerd en interferentie-robuuste radiocommunicatiesysteem voor WSN’s. Bijzondere aandacht wordt geschonken aan de ontvanger. Immers, de ontvanger staat meestal de hele tijd aan om mogelijke signalen van de zender te ontvangen. De ontvanger is het bepalende deel in de prestaties van de radio. Optimalisatie van de radio op systeemniveau wordt uitgevoerd en nieuwe technieken worden voorgesteld om het stroomverbruik van de ontvanger te reduceren.

Om het energieverbruik van een duty-cycle-WSN-radio te verminderen, wordt een optimalisatie methode voorgesteld die de fundamentele systeemrelaties combineert. Deze nieuw geïntroduceerde werkwijze leidt tot een optimale keuze van ruisgetal en datasnelheid voor bepaalde toepassingen en gekozen radio architectuur. In dit proefschrift wordt aan de hand van een reeks van typische radio parameters aangetoond dat het energieverbruik ingerdaad kan worden verminderd met ongeveer 30%. Bovendien is deze werkwijze ook
effectief voor 'duty-cycle wakeup radio’s (radio’s die in slaap-mode gaan gedurende lange
tijd om energie te besparen).

In de meeste radio architecturen wordt het meeste vermogen verbruikt in de kwadratuur
frequentiedelers. Om het stroomverbruik te verminderen, met behoud van een lage
output jitter, moeten de flipflops in de frequentiedelers zorgvuldig gekozen worden.
Een analytische vergelijking is uitgevoerd tussen twee typen flipflops, de dynamische
transmissiepoort logica DTGL (dynamic transmission gate logic) en de stroom domein
logica i.e. CML (current mode logic). Uit deze vergelijking blijkt dat de DTGL flipflop een
lager stroomverbruik heeft voor het beoogde frequentiebereik in het 90 nm CMOS-proces.

Om de storingsrobuustheid te verbeteren wordt een chirped-LO spread spectrum
modulatie techniek voorgesteld voor FSK en PSK radio systemen. De chirped-LO spread
spectrum techniek heeft in vergelijking in andere spread spectrum technieken als voordeel
een ultra laag energieverbruik met een eenvoudige ontvangerarchitectuur. Uit analyse van
het chirped-LO systeem blijkt dat de bit error ratio (BER) van de chirped-LO-systemen
beter is dan de overeenkomstige niet ge-chirped systemen wanneer de storingsfrequentie
nabij de draaggolffrequentie ligt. Het interferentiepatroon van chirped-LO systemen is
onafhankelijk van de storingsfrequentie. Simulatieresultaten bevestigen deze analyse.

Uit de BER analyse van een chirped-LO directe conversie FSK ontvanger blijkt dat de
in-band interferentie robuustheid (de interferentie signaal verhouding (ISR)), kan worden
verhoogd door een hogere chirp bandbreedte en een gering aantal databits in een chirp.
Om het energieverbruik van de ontvanger te verminderen, is een nieuwe 3-fase direct
conversie ontvanger architectuur, ontworpen samen met een laag vermogen demodulator.
De ontvanger, gefabriceerd in 65 nm CMOS technologie, met een datarate van 8 Mbps en
een gevoeligheid van -70 dBm bij een BER van $10^{-3}$, verbruikt slechts 219 $\mu W$ in continu
mode met een 1,2 V voeding op een HF frequentie van 2,45 GHz. Dit komt overeen met een
energie-effiïentie van 27 pJ/bit, drie keer beter dan de eerder gepubliceerde ontvangers.

In de chirped-LO-modus, met een spread spectrum bandbreedte van 360 MHz, kan de
ontvanger een BER bereiken van $10^{-3}$, bij een storing/signaal verhouding van 8 dB over het
gehele frequentiebereik met slechts 15 $\mu W$ aan extra vermogen en een gevoeligheid afname
van minder dan 4 dB. Deze storingsrobuustheid is 13,5 dB hoger dan eerder gepubliceerde
interferentie robuuste ultra low power ontvangers.

De ultra lage energie technieken die worden voorgesteld in dit proefschrift kunnen
in WSN radio’s worden toegepast om zodoende een aanzienlijke verbetering van
de levensduur van de batterij van een sensor node te realiseren. De voorgestelde
storingsonderdrukking techniek kan worden toegepast om de robuustheid van draadloze
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Chapter 1

Introduction

Wireless communication has been a major driving force to improve human life by its technological advancements. The discovery of electromagnetic waves [1] enabled major scientific inventions throughout the last century. Those discoveries have resulted in break-through applications which were almost unthinkable before. The world we live in today is largely dependent on the wireless communication techniques that has been developed. Other than communications technologies such as cellular telephony, internet, satellite communication, near field communication (NFC), and audio/video broadcasting, wireless technology has also given a major boost to numerous other scientific fields such as airplane/ship navigation, object detection systems, medical systems, Global Positioning Systems (GPS), cooking ovens and home and industry automation. Table 1.1 shows the major wireless standards, their frequency of operation and related applications to get a glimpse of the most important wireless technologies that are being used today[2].

Sensors are also being used more and more to connect the physical world with the digital world and thereby increase the intelligence and interfacing capabilities of an electronic system. For example, an airplane today uses at least 10s to 100s of sensors to improve performance and safety. With technology advancement of Micro-Electro Mechanical System (MEMS) and CMOS, more and more sensors can be manufactured in miniaturized form. This enables the development of tiny devices with environmental sensors for intelligent systems.

Integrated Circuits (IC) technology, invented in the 1950s [3], has enabled the miniaturization of high performance electronics. The core performance of most modern electronic devices is dictated by a few small ICs invisible inside packages. IC technology has come through a tremendous advancement over the last half a century. Using integrated CMOS technology with its scaling advantages, computer microprocessors and memories
have achieved several orders of magnitude improvement in power, performance and size over the last decade. The miniaturization and performance improvement facilitate complex communication systems to be integrated in a single IC called System on Chip (SoC).

1.1 Wireless sensor networks

Fueled by the growth of IC, sensor and wireless communication technologies, Wireless Sensor Networks (WSNs) target various breakthrough applications [4, 5]. A WSN consists of numerous devices, called sensor nodes (SN), distributed in a specific area, able to sense and process data and communicate without wires. The sensor nodes are able to communicate with each other and perform together an intelligent task based on the environmental conditions obtained by a set of sensors. Sensor nodes could be placed randomly in a targeted area, which could be for example a building, a cultivation field,
a road, an ocean or a forest. The sensors sense the environmental conditions (such as temperature, light, vibration, location, gas and chemical composition) and store them. A simplified WSN layout is shown in Figure 1.1. As shown in the figure, there is a special type of node called gateway node to collect the data from multiple sensor nodes and process them together. A sensor node communicates its data to a gateway node either directly or via another sensor node(s). For some applications, the gateway nodes collect all data and take decisions based on the data. In some other applications the gateway node transmit the data to a base station controlled by a human or a machine. The position of the sensor nodes can be either random, predetermined or dynamic, depending on the applications and the available hardware.

Figure 1.1: A typical wireless sensor network

1.1.1 Applications of WSNs

WSNs have the potential to be applied in a variety of applications such as medical, disaster management and prevention, home automation, tracking and remote sensing. The application area is huge and one can imagine numerous new applications which will improve human life or prevent disasters in the future. These applications are possible in the future provided that low energy consuming, tiny, cheap and scalable sensor nodes with a robust sensor network are available. Here, some of the applications of WSNs are described.

1. Medical applications: There is a rising demand for WSNs to revolutionize and automate the medical process and equipment. Monitoring the condition of elderly patients and being able to alert health problems or accidents to a doctor or others can save time and also drastically reduce time for treatment. A similar approach can be
used to monitor persons having long term diseases like high blood pressure and high blood sugar. A WSN around and in the human body which can do multiple sensing tasks by various distributed sensors is called a Body Area Networks (BAN) and it is currently a very active field of research [6].

2. **Building management and industry management:** Building management is one of the key applications of sensor networks where some practical working systems are already in place [7]. Energy optimization of a building can be accomplished by automatically switching ON/OFF lights, air-conditioners (based on room temperature) etc. Building security can be enhanced by intruder tracking and movement detection.

In industry, many processes need to be checked and quality controlled which can be executed by a WSN saving expensive human interventions. Automatic environmental control, machine health monitoring and process control are some of the other applications of WSNs in an industrial environment.

3. **Remote access and military:** One of the major target applications of a sensor network is to access various environmental conditions from a remote place. There are places which are difficult or time consuming to reach. To obtain information from a remote place, a sustainable WSN can be used without somebody being present. For instance, environmental tracking inside the ocean, big forests, on top of mountains or volcanoes [8] or in space can be achieved by a properly placed sensor network. In military applications, intruder tracking and area monitoring can be accomplished by a smart sensor network without sending somebody to the targeted location. These kind of networks demand fault tolerant sensor nodes with very long battery life.

4. **Disaster detection, control and help:** Another very important WSNs application is disaster detection, such as fires, earthquakes/tsunamis, flood/land-slide, storms. Detection is performed by sensors that measures temperature, light, gas, vibration, acceleration etc. Disaster control can also be achieved by studying disaster characteristics with WSNs and then predicting the possible disaster based on environmental sensing. WSNs can also reduce loss and help recovery when a disaster happens. For example, a WSN formed by sensor nodes attached to firefighters can acquire and communicate the knowledge of fire positions to the firefighters present at different parts of a building which caught fire [9]. This makes a collaborative network among firefighters which can help them save more lives with lower risk.
5. **Others**: There are several other possible applications of WSNs. Some of them are: human machine interface, automatic traffic control for cars/trains/airplane, study animal behavior, agriculture monitoring, structure monitoring of bridges and tall buildings, coal mines stability, smart computer interfaces, virtual games, mind controlled computer interface.

![Diagram of Wireless sensor network in a flower auction](image)

**Figure 1.2**: A proposed application of Wireless sensor network in a flower auction [10]

### 1.1.2 Use case

To show a practical WSN application and associated requirements and challenges, a use case is defined and illustrated in this subsection.

A possible example application scenario for a WSN is logistics in an industrial environment. A large economic sector in the Netherlands is the 'flower sector'. The logistic process starts from flower auction to customer delivery. Controlling the environment of the flower at difference stages of the auction to customer delivery is a complex and expensive task. A desirable scenario of the flower industry process flow using an efficient WSN is shown in Figure 1.2 [10].

The process from a flower auction to the customer delivery is tracked by a sensor network. The flowers are first auctioned and sold in the Auction-Hall (left side of the figure)
and then kept in a ‘Reticle’ equipped with sensor node(s). Since flowers are sensitive to environmental conditions, a sensor node will consist of sensors sensing temperature, light, pressure and location etc. After that the Reticles are stored in a big room called 'Expedition floor' before sending them to their corresponding customers. The transportation of the Reticles to the customer is carried out by a Trailer (right side of the figure). At the customers place, the sensor nodes can be switched off after the data is sent to a loading gate situated at the trailer. The Reticles are returned from the customers place when the flowers are delivered. Other than the sensor nodes in the Reticle, there are also infrastructure sensor nodes and data-collector nodes to help to collect and analyze sensor data. The infrastructure nodes are shown by blue squares and the data-collector nodes are shown by the yellow triangles in the figure.

Throughout the process, the condition of the flowers is tracked to ensure good quality and also provide detailed knowledge in case of problems. In a long logistic process chain, quality control is often a major challenge. An even bigger challenge is to find out the reason in case of quality degradation. The WSNs can provide an automatic solution for these problems and even it can perform more operations like:

1. Give information to the supplier/trailer driver about the customer and its address to help delivery, if the correct data is stored in the nodes just after the auction.
2. Track the whole supply chain to avoid any mistake and reduce manual work.
3. Customers can check the environment of their ordered flower throughout the process of storage and delivery.
4. The loading and unloading of flower Reticles to and from the expedition floor can be smarter by having WSNs providing information about the order in which flowers/Reticles are needed to move in or out.

Similar logistic control by WSNs can also be applied to the logistics of various other products which needs to be quality controlled.

The following specifications are derived from this user case.

1. **Communication distance**: The sensor has to communicate to other sensor nodes or gateway nodes in the Expedition floor and in the trailer. In the trailer, the distance requirement is $< 5 \text{ m}$. In the expedition floor, there are infrastructure nodes (gateway nodes) evenly placed. The range, the nodes need to be to enable communicate, is therefore limited to 5 meters. Although most WSNs applications target for comparatively higher communication distance, the requirement is kept low here to
1.1. Wireless sensor networks

have advantages like more probability of line of sight (LOS) communication and potentially reduce power consumption by using multi-hop [11] for higher distance communication.

2. **Frequency of operation:** As sensor networks operate in short range and target low cost, an unlicensed band of frequency is generally used for a WSN. To use an unlicensed band, an ISM band must be chosen. For high frequencies, the antenna size can be small, but the transceiver power consumption increases [12]. On the other hand, for low frequencies a larger antenna size is needed which increases the sensor node size. As a tradeoff, The ISM band around 2.45 GHz is chosen as a carrier frequency for communication in a LOS channel.

3. **Power consumption requirement:** The power consumption of a sensor node has to be small to guarantee a long life time using a cheap and small battery with no maintenance or recharging. The battery size of a sensor node is limited by the allowed volume of the node. To keep the sensor node size low (for example within 10 cm$^3$), and to have low cost, a cheap AAA battery with a volume of 4 cm$^3$ can be used. Assuming an energy density of around 250 mWh/cm$^3$ [13], the average power consumption of the entire sensor node should be less than $250 \cdot 10^{-3} \cdot 4/(5 \cdot 365 \cdot 24) = 22.2 \mu W$ to achieve a life time of 5 years. Assuming half of the entire node energy is available to the transceiver (TRX) to consume, TRX has to operate with only $11 \mu W$ of average power.

To meet this ultra low average power requirement, an ultra low power transceiver as well as an effective Medium Access Control (MAC) protocol is necessary. In the MAC protocol, an effective solution is to duty cycle the transceiver [11]. In this method the transceiver is switched ON for the required communication time and then switched OFF to reduce power consumption. Because of the requirement of low average data transmission rate over a fixed time in WSNs applications, the transceiver can be switched OFF for most of the time. In this thesis, unless otherwise mentioned, ‘power consumption’ indicates/represents ‘ON mode power’, and ’average power consumption’ indicates/represents the power averaged over both ON and OFF mode. Similarly energy-per-bit performance indicates only ON mode energy divided by the number of bits, and ’average energy-per-bit’ indicates ON-OFF mode energy together divided by the number of bits. The term ‘ultra low power’ is used in the thesis to specify the technical area where the power or energy consumption is pushed to extremely low or the minimum possible.
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The reduction of ON mode and average energy-per-bit (or energy for a given number of bits) is the goal of this thesis. However, power consumption while the TRX is ON is also important and has to be reduced so that the WSNs can operate by energy harvesting schemes [14], preferably in the range of 100 \( \mu \text{W} \).

1.2 Sensor node survey

In this section, a literature survey of components and blocks used by existing sensor nodes is provided. In Table 1.2, existing Commercial Off-The Shelf (COTS) sensor nodes are compared. The type of radio, microprocessor, memory, battery, size and total power consumption corresponding to each of the nodes are given. As an example, Figure 1.3 shows a sensor node developed by Devlab [15]. Most of these sensor nodes are optimized for power consumption. However, the power is still much higher than the application’s demand.

Table 1.2: Selected existing sensor node comparison

<table>
<thead>
<tr>
<th>Node names</th>
<th>Company/University</th>
<th>Radio</th>
<th>Processor</th>
<th>Memory (Program/External)</th>
<th>Battery</th>
<th>Size [mm]</th>
<th>Total power (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MICA2 [16]</td>
<td>Crossbow</td>
<td>Chipcon CC1000</td>
<td>Atmega 120L</td>
<td>4K/128K flash</td>
<td>2 AA</td>
<td>58x32x7</td>
<td>165</td>
</tr>
<tr>
<td>BTnode v3</td>
<td>ETH Zurich</td>
<td>Chipcon CC1000</td>
<td>Atmega 120L</td>
<td>244K/128K flash</td>
<td>2 AA</td>
<td>58x33</td>
<td>102/198</td>
</tr>
<tr>
<td>Sun spot</td>
<td>Sun microsystem</td>
<td>TICC2420</td>
<td>ARM 920T</td>
<td>512K/4M</td>
<td>lithium-ion</td>
<td>41x23x70</td>
<td>100</td>
</tr>
<tr>
<td>EyesIFX v2</td>
<td>TU Berlin</td>
<td>Infenion TDA 5150</td>
<td>RISC processor</td>
<td>10K/48M</td>
<td>-</td>
<td>-</td>
<td>72</td>
</tr>
<tr>
<td>Tiny node</td>
<td>EPFL</td>
<td>Samtech SX1211</td>
<td>RISC processor</td>
<td>101K/12K</td>
<td>2x AA</td>
<td>30x40</td>
<td>-</td>
</tr>
<tr>
<td>IMOTE v3</td>
<td>Crossbow</td>
<td>TICC2420</td>
<td>MMX DSP co-processor</td>
<td>256K/32M</td>
<td>3x AA</td>
<td>36x48x9</td>
<td>66</td>
</tr>
<tr>
<td>Mule v3</td>
<td>Lulea University</td>
<td>Mitumi C46AH</td>
<td>Renesas M16C62P</td>
<td>31K/392K + 2M EEPROM</td>
<td>1 Lishen Lithium-polymer</td>
<td>26x24x5 x 0.25</td>
<td>48</td>
</tr>
<tr>
<td>Iris [23]</td>
<td>MEMSIC</td>
<td>Atmel AT86RF230</td>
<td>Atmel ATMega 1281</td>
<td>8K/512K</td>
<td>2x AA</td>
<td>2.25 x 1.25 x 0.25</td>
<td>41</td>
</tr>
<tr>
<td>MyriaMode</td>
<td>DevLab</td>
<td>Nordic Semiconductor NRF24L01P</td>
<td>EnergyMicro EFM32G230F</td>
<td>2x AAA</td>
<td>53x58x18 mm</td>
<td>-</td>
<td></td>
</tr>
</tbody>
</table>

More detailed sensor node survey can be found in, for example [24], [19] and [25]

Table 1.3 shows the power consumption breakdown of the sensor nodes. The TRX power contribution is written in the last column. This is also the TRX energy consumption
assuming the TX, RX and microprocessors are ON during the same time. As can be seen, a large part of the power is consumed in the sensor node transceiver (TRX) block for radio communication. Therefore, it can be concluded that to reduce energy consumption of a sensor node significantly, the TX and RX energy consumption has to be reduced.

Figure 1.3: A sensor node by Devlab: MyriaModem [15]

Table 1.3: Existing sensor node survey; Power consumption break down

<table>
<thead>
<tr>
<th>Node names</th>
<th>RX Power</th>
<th>TX Power</th>
<th>Microprocessor power</th>
<th>Total power</th>
<th>TRX power contribution</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unit</td>
<td>10 [mW]</td>
<td>27 [mW]</td>
<td>8 [mW]</td>
<td>45 [mW]</td>
<td>82 %</td>
</tr>
<tr>
<td>MICA2</td>
<td>52 [mW]</td>
<td>57 [mW]</td>
<td>62 [mW]</td>
<td>171 [mW]</td>
<td>64 %</td>
</tr>
<tr>
<td>Sun spot</td>
<td>28 [mW]</td>
<td>36 [mW]</td>
<td>7.2 [mW]</td>
<td>72 [mW]</td>
<td>88 %</td>
</tr>
<tr>
<td>EyesIFX v2</td>
<td>41 [mW]</td>
<td>142 [mW]</td>
<td>6.3 [mW]</td>
<td>230 [mW]</td>
<td>79 %</td>
</tr>
<tr>
<td>Tiny node</td>
<td>-</td>
<td>175 [mW]</td>
<td>18 [mW]</td>
<td>203 [mW]</td>
<td>86 %</td>
</tr>
<tr>
<td>IMOTE</td>
<td>-</td>
<td>175 [mW]</td>
<td>18 [mW]</td>
<td>195 [mW]</td>
<td>44 %</td>
</tr>
<tr>
<td>Mulle v3</td>
<td>-</td>
<td>175 [mW]</td>
<td>18 [mW]</td>
<td>203 [mW]</td>
<td>86 %</td>
</tr>
<tr>
<td>Iris</td>
<td>48 [mW]</td>
<td>39 [mW]</td>
<td>24 [mW]</td>
<td>111 [mW]</td>
<td>78 %</td>
</tr>
</tbody>
</table>
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1.2.1 Sensor node architecture

A typical sensor node architecture is shown in Figure 1.4. It consists of a wireless TRX which can communicate with other sensor nodes, and the gateway node(s). A set of sensors sense the environmental condition periodically. Sensor data is converted to the digital domain by an Analog to Digital Converter (ADC) before being stored in memory. There is a micro-processor to process the data. There are two types of memory needed for a sensor node; one which stores the data (even in sleep mode) and another which is randomly accessible by the microprocessor so that it can run the application program. There is a battery and power management unit. The radio communication part of the sensor node is highlighted. It consists of a receiver, transmitter, modem, coding-decoding and some digital processing.

1.2.2 Major challenges of sensor nodes

1. **Energy consumption:** As the sensor node battery cannot be recharged or replaced periodically for most WSNs applications, the lifetime of the nodes has to be very high [26]. Therefore the energy consumption of the sensor nodes has to be very low, otherwise a large battery size in a sensor node will make the nodes bulky and unsuitable for most WSNs applications. Another attractive option is to use energy harvesting technology so that the nodes can function without batteries. However, to
Table 1.4: Major challenges of WSN and target communication layer(s)

<table>
<thead>
<tr>
<th>Challenges</th>
<th>Target communication layer</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low energy consumption</td>
<td>all</td>
</tr>
<tr>
<td>Reliability and robustness</td>
<td>physical, network</td>
</tr>
<tr>
<td>Cost</td>
<td>all</td>
</tr>
<tr>
<td>Size of the nodes</td>
<td>physical</td>
</tr>
<tr>
<td>Usability and standardization</td>
<td>all</td>
</tr>
<tr>
<td>Network scalability</td>
<td>network</td>
</tr>
</tbody>
</table>

2. **Robustness:** The wireless communication has to be robust enough to interferences so that sensor data can be transferred reliably. Because WSNs may have to operate in an unlicensed and overly crowded ISM frequency band, interference robustness is very critical.

3. **Cost:** The cost reduction of the sensor node is a big challenge as well because traditional wireless transceiver circuits need high-cost technologies and discrete components.

4. **Size:** Another big challenge of WSNs is that the sensors should have a very small size (ideally like a dust particle!), so that they can be placed in the environment without being noticeable or at-least without occupying extra space. It is more difficult to achieve along with the lifetime requirement, because a large battery is needed for higher lifetime. Battery size has not been scaling down as good as the ICs [26].

5. **Standardization:** Standardization is another challenge; it is difficult to use a single standard for all WSN because of the variety of scenarios. For example, the distance requirement for remote access and medical applications can be highly different.

Other challenges of WSNs are network scalability and fault tolerance which should be targeted in the higher layers of the Open System Interconnection (OSI) model.  

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1There are seven layers in a OSI model. From top to bottom they are 1. Application layer, 2. Presentation layer, 3. Session layer, 4. Transport layer, 5. Network layer, 6. Data link layer, 7. Physical layer.
Table 1.4 shows the major challenges of a sensor network along with the target communication layer. The first two challenges in the table, i.e. low energy consumption and communication reliability and robustness are the bottlenecks for the WSNs application and commercialization and they are limited by the the TRX. In this thesis, solutions for these two challenges are proposed.

1.3 Radio communication for WSNs

As the major challenges of a sensor node must be addressed by targeting the radio communication part of a sensor node, the focus of this thesis will be on the transceiver (TRX). A survey and comparison of commercially available TRXs are given in Table 1.5.

1.3.1 Commercial WSNs radio

As we can see in Table 1.5, the power consumption of TRX does not satisfy our requirement and needs a reduction by more than two orders of magnitude. The transceiver with lowest power consumption needs an operating power of more than 15 mW, whereas the maximum power allowed is in the range of 100 $\mu$W in case of energy harvesting radios without energy storage. Although the average power of some existing transceiver are already less then $\mu$W range depending on the duty-cycling factor, the ON mode power should be reduced to support energy harvesting and also to increase the battery life further. Another observation is that in general the TRXs use simple binary modulation schemes such as the Binary Frequency Shift Keying (BFSK), On-Off Keying (OOK) or Amplitude Shift Keying (ASK) for communication communication because these applications have relaxed BER and data-rate performance requirements and to save power consumption.
<table>
<thead>
<tr>
<th>Radio</th>
<th>Chipcon CC1100</th>
<th>TI CC2420 SX1211</th>
<th>Infineon TDA5250</th>
<th>Microchip MRF89XAN</th>
<th>Mitsumi C46AHR</th>
<th>Microsemi ZL70250</th>
<th>Atmel AT86RF230</th>
<th>RFM TR1003</th>
<th>TI CC2520</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bit rate [Kbps]</td>
<td>1.2-500</td>
<td>250</td>
<td>200</td>
<td>64</td>
<td>16-40</td>
<td>1000</td>
<td>186</td>
<td>250</td>
<td>200</td>
</tr>
<tr>
<td>Modulation</td>
<td>FSK/GFSK/OOK/ASK</td>
<td>DSSS on O-QPSK</td>
<td>FSK/ASK</td>
<td>FSK/OOK</td>
<td>FHSS, GFSK</td>
<td>GFSK</td>
<td>OQPSK</td>
<td>FSK/OOK/</td>
<td>DSS</td>
</tr>
<tr>
<td>Output power [dBm]</td>
<td>-9/10</td>
<td>0-24</td>
<td>10</td>
<td>13</td>
<td>-9 to 10</td>
<td>0</td>
<td>-13 to -2</td>
<td>-17 to 3</td>
<td>-4 to 11</td>
</tr>
<tr>
<td>BER</td>
<td>$10^{-3}$</td>
<td>$10^{-3}$</td>
<td>$10^{-3}$</td>
<td>$10^{-3}$</td>
<td>$10^{-3}$</td>
<td>$10^{-3}$</td>
<td>$10^{-3}$</td>
<td>$10^{-2}$</td>
<td>$10^{-2}$</td>
</tr>
<tr>
<td>Supply voltage [V]</td>
<td>3V (1.8 - 3.3)</td>
<td>3.3</td>
<td>3.3</td>
<td>3 (2.1-5.5)</td>
<td>3.3 (2.1-3.6)</td>
<td>1.8-3.6</td>
<td>1.1-1.9</td>
<td>1.8 to 3.6</td>
<td>2.1 - 3.6</td>
</tr>
<tr>
<td>RX Current consumption [mA]</td>
<td>14.4</td>
<td>18.8</td>
<td>3</td>
<td>8.6/9</td>
<td>3</td>
<td>15</td>
<td>1.9</td>
<td>15.5</td>
<td>1.8</td>
</tr>
<tr>
<td>TX Current consumption [mA]</td>
<td>13/31</td>
<td>17.4</td>
<td>25</td>
<td>12/13.3</td>
<td>25</td>
<td>17</td>
<td>5</td>
<td>16.5</td>
<td>12</td>
</tr>
<tr>
<td>Total Power consumption [mW]</td>
<td>80/130</td>
<td>108</td>
<td>84</td>
<td>63</td>
<td>84</td>
<td>96</td>
<td>10.35</td>
<td>96</td>
<td>41.4</td>
</tr>
<tr>
<td>Standby power [µA]</td>
<td>0.4</td>
<td>NA</td>
<td>0.1</td>
<td>0.1</td>
<td>0.6</td>
<td>0.5</td>
<td>0.02</td>
<td>0.1 to 1</td>
<td>1</td>
</tr>
<tr>
<td>Startup time [µs]</td>
<td>90</td>
<td>100</td>
<td>100</td>
<td>500</td>
<td>NA</td>
<td>NA</td>
<td>3000</td>
<td>NA</td>
<td>200</td>
</tr>
<tr>
<td>Standard</td>
<td>NA</td>
<td>IEEE 802.15.4</td>
<td>NA</td>
<td>NA</td>
<td>Bluetooth</td>
<td>NA</td>
<td>IEEE 802.15.4</td>
<td>102.15.4</td>
<td>NA</td>
</tr>
</tbody>
</table>

1 at 1.5 V power supply for the Microsemi ZL70250, and 3 V power supply for the rest.

NA=Not available.
1.3.2 Reported WSNs radios receivers

As the wireless receiver often needs to be ON for most of the time or even always-ON, whereas a TX needs to operate only while active, the receiver power consumption contributes more to the overall TRX energy consumption. Moreover, the RX is often more critical in terms of overall TRX interference robustness. Therefore, low power and interference robust receiver design is the primary target of this thesis. The performance of recently reported receivers in literature are listed in Table 1.6. As can be seen, most of these receivers operate at low data rate to minimize operating power consumption except [28], where lowest energy per bit of 84 pJ/bit is achieved by using 5 Mbps at 920 MHz. A lower energy per bit is desirable to achieve higher battery lifetime for the WSNs. The reported radios, both commercial or published could be duty-cycled. However, the radios which are targeted for energy-per-bit performance instead of just targeting power consumption are truly energy optimized for duty-cycled systems.

Most of the ultra low power/energy transceivers use simple modulation schemes and less selective front-end architectures which are interference sensitive. Among the ultra low power receivers, only [29] reports interference robustness compared to conventional receivers. It supports maximum 20 dB of interference to signal ratio (ISR). The ISR, across all interferer frequency range (including in-band), however is only -5.5 dB. These performances of interference robustness and energy efficiency of wireless receivers need to be enhanced to facilitate more WSN applications.

To address the requirement of an always-ON receiver, a low power separate receiver called ‘wakeup’ receiver [30] has been proposed. The wakeup receiver is now always-ON and the main receiver is duty-cycled. The wakeup receiver senses the channel for a incoming signal and wakes up the main receiver only when it needs to operate.

1.3.3 Transceiver energy reduction challenges

The target of energy reduction of a wireless TRX is not new. It has been a primary objective for most TRXs designed to be used in mobile and hand-held communication devices. Also, research and development on low power/energy TRXs for WSNs has been going on throughout the last decade. Yet, the transceiver power reduction achieved is less compared to the power reduction achieved in other sensor node blocks such as the microprocessor and semiconductor memories. There are several reasons why the power minimization of a transceiver is very difficult, especially while keeping the receiver robustness intact. Power consumption of digital circuits has significantly reduced as a result of CMOS technology
1.3. Radio communication for WSNs

Table 1.6: Receiver performance summary and comparison

<table>
<thead>
<tr>
<th>Author [Ref]</th>
<th>Tech. Power Supply</th>
<th>Frequency MHz</th>
<th>Data-rate Kbps</th>
<th>Sensitivity dBm</th>
<th>Power µW</th>
<th>Modulation</th>
<th>Area mm²</th>
<th>SIR MIN</th>
<th>Energy pJ/bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Huang, [29]</td>
<td>90 1.2</td>
<td>915</td>
<td>10</td>
<td>-83</td>
<td>121</td>
<td>OOK</td>
<td>1.27</td>
<td>-5.5</td>
<td>1200</td>
</tr>
<tr>
<td>Bae, [28]</td>
<td>180 0.7</td>
<td>920</td>
<td>5000</td>
<td>-73</td>
<td>420</td>
<td>FSK</td>
<td>-</td>
<td>-</td>
<td>84</td>
</tr>
<tr>
<td>Cook, [31]</td>
<td>130 0.4</td>
<td>2400</td>
<td>500</td>
<td>-100</td>
<td>330</td>
<td>FSK</td>
<td>-</td>
<td>-</td>
<td>1100</td>
</tr>
<tr>
<td>Fletcher, [32]</td>
<td>90 0.5</td>
<td>2000</td>
<td>100</td>
<td>-72</td>
<td>52</td>
<td>OOK</td>
<td>0.1</td>
<td>-</td>
<td>500</td>
</tr>
<tr>
<td>Daly, [33]</td>
<td>180 0.5</td>
<td>2000</td>
<td>100</td>
<td>-65</td>
<td>2500</td>
<td>OOK</td>
<td>0.27</td>
<td>-</td>
<td>2500</td>
</tr>
<tr>
<td>Pandey, [34]</td>
<td>130 1</td>
<td>400</td>
<td>200</td>
<td>-70</td>
<td>44</td>
<td>FSK</td>
<td>0.5</td>
<td>-</td>
<td>220</td>
</tr>
<tr>
<td>Moszzeni, [35]</td>
<td>130 1/0.5</td>
<td>915</td>
<td>200</td>
<td>-75</td>
<td>22.9</td>
<td>OOK</td>
<td>0.2</td>
<td>-</td>
<td>110</td>
</tr>
<tr>
<td>Bae, [36]</td>
<td>180 0.7</td>
<td>80</td>
<td>312</td>
<td>-62</td>
<td>45</td>
<td>FSK</td>
<td>1</td>
<td>-</td>
<td>140</td>
</tr>
<tr>
<td>Zgaren, [37]</td>
<td>130 1.2</td>
<td>902-928</td>
<td>8000</td>
<td>-78</td>
<td>639</td>
<td>FSK</td>
<td>0.49</td>
<td>-</td>
<td>80</td>
</tr>
</tbody>
</table>

∗ SIR MIN is minimum signal to interference ratio required to achieve $BER = 10^{-3}$; indicates the interference robustness of these receivers.

scaling. Table 1.7 shows the effect of technology scaling on the important parameters [38]. As shown in the right side (last 3 columns) of the table, CMOS downscaling reduces MOS transistor drain current, area, capacitance and switching power consumption even at increased speed. The digital circuit power consumption ($P = \alpha_{SW}CV^2f$) is reduced by the scaling factor to the power three. Although this type of ‘simple’ scaling has stopped in very modern technologies (smaller then 20nm), still power is reduced while migrating to a smaller node.

On the other hand, for analog/RF circuit designs the situation is completely different. Except for component matching limited blocks, analog circuits face several consequences such as lower signal to noise ratio (SNR) and lower dynamic range due to the technology and supply voltage scaling [39] and more power needs to be consumed to compensate voltage scaling for noise limited circuits. Because of the domination of large digital blocks in most modern systems, CMOS technology scaling and supply voltage scaling is usually targeted for SoCs. Therefore there is a need for transceiver architectures and circuits which are both low power and have a trend to reduce power consumption with the technology scaling.

1.3.4 Interference robustness challenges in low power transceiver

The interference robustness of TRX is often ignored in WSNs radio design. The communication of most WSNs has to happen in the very crowded ISM frequency bands [27]. The global ISM band in the frequency range from 2.4 GHz to 2.5 GHz is widely
Chapter 1. Introduction

Table 1.7: CMOS technology scaling advantages on the digital performance [38]

<table>
<thead>
<tr>
<th>Scaled Parameters</th>
<th>Before scaling</th>
<th>After scaling</th>
<th>Performance Parameters</th>
<th>Before scaling</th>
<th>After scaling</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel length</td>
<td>L</td>
<td>L/\frac{2}{3}</td>
<td>Drain current, ( I_d = \mu C_{OX} W \frac{(V_{DD} - V_{TH})^2}{2L} )</td>
<td>( I_d )</td>
<td>L/\frac{2}{3}</td>
</tr>
<tr>
<td>Oxide thickness</td>
<td>( t_{OX} )</td>
<td>( \frac{t_{OX}}{S} )</td>
<td>Area, ((A = WL))</td>
<td>( A )</td>
<td>( \frac{A}{S} )</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>( V_{DD} )</td>
<td>( \frac{V_{DD}}{S} )</td>
<td>Gate capacitance, ((C_G = C_{OX}WL))</td>
<td>( C_G )</td>
<td>( \frac{C_G}{S} )</td>
</tr>
<tr>
<td>Threshold voltage</td>
<td>( V_{TH} )</td>
<td>( \frac{V_{TH}}{S} )</td>
<td>Gate delay, (( t_p = \frac{LC_{OX}V_{DD}}{2V_{TH}W(L/W)} ))</td>
<td>( t_p )</td>
<td>( \frac{t_p}{S} )</td>
</tr>
<tr>
<td>MOS width (same W/L)</td>
<td>( W )</td>
<td>( \frac{W}{S} )</td>
<td>Digital power dissipation, (( P = \alpha_{ox}C_GV_{DD}^2f ))</td>
<td>( P )</td>
<td>( \frac{P}{S^2} )</td>
</tr>
<tr>
<td>Mismatch parameter</td>
<td>( A_{VT} )</td>
<td>( \frac{A_{VT}}{S} )</td>
<td>Mismatch error, (( \sigma_{\Delta V_T}^2 = \frac{A_{VT}}{W^2} ))</td>
<td>( \sigma_{\Delta V_T}^2 )</td>
<td>( \frac{\sigma_{\Delta V_T}^2}{S^2} )</td>
</tr>
</tbody>
</table>

chosen for WSNs as a good trade-off between antenna size and power consumption. This frequency band is highly occupied by applications such as WLAN, zigbee, Bluetooth, cordless phone, wireless USB, microwave oven etc (see Table 1.1). The sensor network has to co-exist with one or more of these short range radio applications. A severe effect on TRX performance due to the interference can occur if proper care is not taken [40]. Hence interference robustness against those signals of various standards is necessary for reliable communications between sensor nodes.

A possible interference robust scheme is to use spread spectrum techniques, like Direct Sequence Spread Spectrum (DSSS) [41] and Frequency Hopping Spread Spectrum (FHSS) [42]. The DSSS scheme needs a very high chip rate for a reasonable processing gain and higher data rate [43], which results in higher power consumption in digital processing blocks. In [42], FHSS and DSSS are compared and it was concluded the FHSS has a clear advantage over DSSS in a power constrained system. FHSS however still incurs significant overhead due to the pseudo random code acquisition. Therefore both schemes with their current architectures, are not recommended to be used in ad-hoc networks [44], and there is a challenge for an interference robust mechanism which is also ultra low power.

1.3.5 Motivation of the thesis

The main motivation of this work is to address the two major challenges in state-of-the-art WSNs by targeting the TRX design. These two major challenges are energy reduction and interference robustness for wireless sensor node communication.

To achieve one order of magnitude TRX energy reduction, all sections of the radio design have to be addressed, from device technology, to the TRX system and the MAC protocol level. Cross-layer trade-offs and optimizations need to be done to minimize the energy consumption. Figure 1.5 shows the major aspects which need to be considered
Figure 1.5: Aspects to be considered to reduce power/energy consumption of TRX

to reduce the power consumption of a wireless transceiver. The aspects also can have
trade-offs between each other. These trade-offs have to be considered to achieve minimum
energy.

As mentioned in the previous subsection 1.3.4, there is a requirement of an improved
modulation scheme and TRX architecture to achieve interference robustness at aggressively
low power consumption.

The research question of this thesis is to identify and propose new techniques by
which the radio communication power consumption can be reduced significantly and
communication robustness can be increased.

1.4 Thesis outline

The outline of the thesis is as follows.

In Chapter 2, a power and noise trade-off in a receiver front end is performed for a
given noise figure. This trade-off helps to improve the method to optimize the energy of a
duty-cycled transceiver system. The method provides an optimized choice of noise figure
and data-rate, and improves the overall TRX energy consumption for a given application.
This method is also applied successfully to wakeup receivers. The optimum choice
depends on the MAC protocol used. An example of a wakeup receiver along with a MAC
protocol shows that this approach can indeed improve the energy efficiency of duty-cycled
transceiver system compared to existing common approaches.

Chapter 3, deals with power consumption reduction of a quadrature or other multiphase
frequency divider for a given jitter requirement. The frequency divider is targeted because
it can consume a large part of the quadrature receiver power [45]. Also some applications
need a minimum jitter requirement for a given power. Therefore, a figure of merit is defined based on the admittance scaling of circuit blocks. A comparison is made between Dynamic Transmission Gate Logic (DTGL) flipflops and Current Mode Logic (CML) flipflops based on their power-jitter performance. The flipflop comparison is then used to compare dividers in general for any number of phases. Simulations are used to support the theoretical prediction.

In Chapter 4, a chirped-clock based modulation scheme is proposed to increase the interference robustness of a Frequency Shift Keying (FSK) and a Phase shift Keying (PSK) receiver. Analysis and simulation are used to estimate the bit error ratio (BER) performance in the presence of single tone and partial band interferences. Performance comparison with ideal non-coherent BFSK and BPSK receivers shows that the chirped-LO scheme can improve the receivers interference robustness.

Chapter 5 illustrates the design of an ultra low energy BFSK receiver capable of chirped clock communication. The low power circuit techniques used in the receiver are described. The ultra low energy receiver is fabricated in 65 nm CMOS technology and measurement results are shown. The chirped clock scheme is proven to be interference robust and the performance is insensitive to the interferer frequency. The receiver measurement results also prove the proposed low energy receiver architecture and circuit techniques.

Finally Chapter 6 presents a summary of the thesis and draws its primary conclusions. The original contributions are identified and possible future works and recommendations are provided.

Several chapters in this thesis are based on published work. Chapter 2 is an improved version of [46], Chapter 3 is entirely copied from [47] with minor corrections, Chapter 4 is based on [48] with some additions and improvements and [49] is converted to Chapter 5 after adding some explanations.
Chapter 2

Energy Minimization in Duty-cycled Radio Transceivers

2.1 Introduction

In Chapter 1, the importance and challenges of transceiver (TRX) energy minimization for WSNs applications were highlighted. With that aim, TRX system energy optimization is targeted in this Chapter exploiting fundamental TRX system trade-offs. The energy optimization is targeted at a duty-cycled TRX which is generally employed in ultra low power WSNs. The noise vs. power consumption tradeoff of a TRX circuit used in this chapter assumes a noise limited scenario where interference does not take a performance limiting role. Later in the thesis, in Chapter 4, interference effects and improvement of the robustness is addressed. The core part of this chapter is taken from [46]. Some corrections and improvements were done in the text, and a section which deals with low-power short range systems is added.

In a non-duty-cycled TRX, one general optimization approach is to optimize the transmitter (TX) output power to minimize the total power consumption in the transceiver system. An optimum TX power is required because very high radiated power increases the TX power considerably more than the power reduction achieved by exploiting relaxed sensitivity requirement at the receiver (RX). On the other hand, at very low TX radiated power, the RX consumes much more power to increase its sensitivity. So, there is an optimum level of TX output power, which will minimize the total transceiver power consumption. For a given bandwidth and signal to noise ratio (SNR) requirement in an RX, the RX noise figure (NF) determines the RX sensitivity, and hence the TX minimum output power level for a given link budget. Assuming a fixed LNA noise figure to dissipation
relation, there is an optimum NF corresponding to the minimum total power.

As mentioned in Chapter 1, duty-cycling the radio transceiver is an effective way to reduce the energy consumption [11] in a radio communication system. In a duty-cycled radio, there is another trade-off between duty cycle and datarate [50, 51, 52]. Unless otherwise mentioned, in this thesis 'datarate' indicates the datarate when the TRX is ON. The overall rate of data transfer including the ON and OFF time is represented by 'average datarate'. The tradeoff shown in [50, 51, 52] suggests an optimum datarate, assuming a fixed RX sensitivity. However, fixing the sensitivity will restrict the combined tradeoff of RX and TX. In this chapter, datarate and NF are optimized together without the sensitivity restriction, which reduces energy compared to the previous approaches. The optimization in this Chapter is done assuming a fixed process technology. To optimize across technologies, the optimization described in this Chapter can be iteratively repeated to obtain minimum energy points across various technologies. This optimization can also be applied to TRXs with other rendez-vous schemes [53]. To show the energy reduction, this approach is applied to two rendez-vous schemes; a synchronous scheme and a pseudo-asynchronous scheme. The example of the pseudo-asynchronous scheme is a slot based MAC protocol [54] proposed for a wakeup radio.

2.2 Transceiver parameters for a minimum energy non-duty cycled radio

![Diagram of wireless transceiver and its noise limitation](image)

Figure 2.1: Wireless Transceiver and its noise limitation
2.2. Transceiver parameters for a minimum energy non-duty cycled radio

In this section, optimization of a non-duty cycled radio is described. Both the RX and TX are assumed to be always ON in this non-duty cycled radio. Although in most of the practical wireless communications, the TX is not always ON, for simplicity here it is not considered. The duty-cycle effects for both RX and TX are analyzed in the later sections. For this radio, the total transceiver power consumption can be written as:

\[ P_T = P_{RX} + P_{TX} \]  \hspace{1cm} (2.1)

where \( P_{RX} \) is RX power consumption and \( P_{TX} \) is TX power consumption. The noise contribution and power consumption can be traded off in the RX front-end blocks, such as mixer, Low Noise Amplifier (LNA) etc. [55]. Typically in an RX front-end, as shown in Figure 2.1, the LNA amplifies the RF signal such that the effect of the rest of the blocks on the RX NF is not very significant for most systems. Therefore RX NF can be assumed to be dominated by the LNA NF, similar to [56]. Unlike most traditional radios, in WSNs applications, the receiver power consumption is also a significant contributor to the total TRX power consumption. Therefore targeting the minimum NF for the RX front end does not necessarily minimize TRX energy consumption. Hence there is a requirement to investigate the noise figure and power consumption trade-off in a receiver. It is assumed here that lowering the noise figure of the RX front-end results in a higher power dissipation. Moreover it is assumed that the RX front-end noise factor \( (F_R) \) is determined by the LNA noise factor \( (F_L) \). Considering a widely used common source LNA, the noise factor and the LNA power can be related as [56],

\[ F_R \approx F_L = 1 + \frac{K_L}{P_L} \]  \hspace{1cm} (2.2)

where \( F_R \) is the receiver noise factor (unit-less), \( F_L \) and \( P_L \) are the LNA noise factor (unit-less) and the power consumption (watt) respectively, \( K_L \) is a design constant, expressed in watt (required power consumption to achieve \( F_L = 2, \) [=3 dB]) which depends on the gain, IIP3, the LNA configuration, technology, etc. It is a trade-off between noise and power consumption assuming other performance parameters are kept fixed (such as IIP3, gain of the LNA etc.). Relation (2.2), which could of course be replaced by a more complicated relation, is assumed throughout this chapter and forms the basis for its results. Another way to arrive at (2.2) is by assuming that an LNA can be designed to achieve a fixed ‘figure of merit’ [FoM1 and FoM2 in [57]] even if its power consumption and NF is varied. In this chapter, Noise factor \( (F) \) is used instead of NF \( [NF = 10.\log_{10}(F)] \) for simplification of calculation, although the NF is specified and discussed in the text as it is
commonly used in RX specification. The rest of the power consumption in the RX, other than LNA, is independent of the RX NF. Therefore, the total RX power consumption can be approximated as,

\[ P_{RX} = P_{Rf} + \frac{K_L}{F_R - 1} \]  \hspace{1cm} (2.3)

where \( P_{Rf} \) is power consumption of the blocks independent of the RX NF, expressed in watt. The TX minimum radiated power is [58]:

\[ P_{RAD} = \frac{SNR \cdot kT \cdot LB \cdot F_R \cdot B}{(G_r \cdot G_t)} \]  \hspace{1cm} (2.4)

where \( SNR \) is signal to noise ratio required in the RX demodulation, \( G_t \) is the TX antenna gain, \( G_r \) is the RX antenna gain, \( B \) is the (noise) bandwidth, \( LB \) is the link budget. The upper value of the link budget is fixed for a given distance and channel property. The \( SNR \) is determined by the demodulator used in the receiver and can have another tradeoff with bandwidth efficiency based on Shannon’s capacity theorem on maximum bandwidth efficiency [59]. This tradeoff is dependent on the channel coding used and for simplicity the \( SNR \) it is assumed to be constant. Thus, the TX power consumption can be modeled as:

\[ P_{TX} = P_{Tf} + \frac{SNR \cdot kT \cdot LB \cdot F_R \cdot B}{\eta G_r G_t} \]  \hspace{1cm} (2.5)

where \( P_{Tf} \) is the transmitter fixed power which is dominated by the oscillator power for most modulation schemes and \( \eta \) = TX power amplifier efficiency. The antenna gains, \( G_r \) and \( G_r \) can be incorporated in the link budget and therefore for simplicity they are assumed to be equal to one. Using (2.5) and the receiver power model of (2.3), the total power consumption of the transceiver system in a peer to peer communication (single-hop) neglecting any overhead addition by the higher layers of communication is obtained as:

\[ P_T = P_{Rf} + \frac{K_L}{F_R - 1} + P_{Tf} + \frac{SNR \cdot kT \cdot LB \cdot F_R \cdot R}{K_{bw} \eta} \]  \hspace{1cm} (2.6)

where \( K_{bw} \) is the bandwidth efficiency defined as the ratio of datarate and bandwidth (as bandwidth is proportional to the datarate for a given spectral efficiency), and \( R \) is the data-rate. \( K_{bw} \) is assumed to be constant and is introduced here to express bandwidth \( B \) in terms of the data rate, \( R \). Differentiating (2.6) with respect to \( F_R \) and equating it to zero,
2.3. Transceiver parameters for energy efficient duty cycled radio

Table 2.1: List of design specification in scenario-I

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Link budget ($LB$)</td>
<td>90</td>
<td>dB</td>
</tr>
<tr>
<td>Signal to noise ratio ($SNR$)</td>
<td>7</td>
<td>dB</td>
</tr>
<tr>
<td>Bandwidth efficiency ($K_{bw}$)</td>
<td>1</td>
<td>(bits/sec)/Hz</td>
</tr>
<tr>
<td>TX power amplifier efficiency ($\eta$)</td>
<td>50</td>
<td>%</td>
</tr>
<tr>
<td>Number of bits per packet ($N_b$)</td>
<td>100</td>
<td>-</td>
</tr>
<tr>
<td>Fixed RX/TX power ($P_{R_f}/P_{T_f}$)</td>
<td>0.5</td>
<td>mW</td>
</tr>
<tr>
<td>Datarate ($R$)</td>
<td>100</td>
<td>kbps</td>
</tr>
<tr>
<td>LNA noise-power constant ($K_L$)</td>
<td>1.52</td>
<td>mW</td>
</tr>
</tbody>
</table>

The minimum power condition is obtained as:

\[
\frac{dP_T}{dF_R} = 0 \implies F_{opt} = 1 + \sqrt{\frac{\eta K_L K_{bw}}{SNR kT LB R}}
\]  

(2.7)

The constant $K_L$ for a specific implementation can be calculated from equation (2.2). As an example, the LNA reported in [57] is chosen, which achieves a NF of 2 dB (i.e. noise factor, $F = 1.58$) and a power consumption of 2.6 mW in a 0.13 µm technology. Using these values in (2.2), the obtained value of $K_L = 1.52 \times 10^{-3}$ watt. Note that $K_L$ can vary with the LNA gain, linearity, technology, frequency of operation etc. For a given scenario, related values are listed in Table 2.1. With the value of $SNR$, $LB$, $K_{bw}$, $\eta$, $K_L$, $R$ from the table, an NF for minimum energy of 14 dB is obtained using (2.7). The change of RX power, TX power and the total power with respect to the NF is plotted in Figure 2.2. It shows that indeed there is an NF value which minimizes the total power consumption. Note that this NF is at one specific datarate chosen as 100 kbps.

2.3 Transceiver parameters for energy efficient duty cycled radio

In this section the TRX parameters are optimized for a duty-cycled radio.

2.3.1 Data rate and duty cycle trade-off for a given receiver sensitivity

In transceivers, power consumption reduces with decreasing datarate because the baseband circuits operate at a reduced frequency [57] and noise bandwidth is less for a given spectral
efficiency. However, for a duty-cycled radio, a higher datarate corresponds to faster transmission and reduced transceiver ON time for a fixed number of bit transmissions, resulting in reduced energy consumption. Therefore, there is a trade-off between datarate and duty cycle. This trade-off has been shown in [11, 51, 52], and used to minimize RX energy consumption. In this section, this approach is incorporated to the total transceiver energy instead of only RX energy. For a fixed sensitivity requirement, if the datarate increases, NF has to be improved to compensate the increase in noise bandwidth. So, if the spectral efficiency is unchanged, the datarate is proportional to the bandwidth and hence inversely proportional to the required noise factor. Therefore,

\[ F_R = \frac{K_{FD}}{R} \]  

(2.8)

where, \( F_R \) is the noise factor of the receiver and \( K_{FD} \) is a design constant, expressed in bps. It can be calculated using a known combination of \( F_R \) and \( R \). The transceiver ON time per packet of \( N_b \) bits is \( \frac{N_b}{R} \), assuming the startup time is negligible. It can be multiplied with a simplified version of (2.6) to get the total transceiver energy in one second as:

\[ E_T = \left( \frac{N_b}{R} \right) \left[ P_{RF} + \frac{K_L R}{K_{FD} - R} + P_{TX} \right] \]  

(2.9)
Table 2.2: List of design specification in scenario-I; Table 2.1 is repeated for convenience and $t_s$ and $P_B$ are added.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Link budget ($LB$)</td>
<td>90</td>
<td>dB</td>
</tr>
<tr>
<td>Signal to noise ratio ($SNR$)</td>
<td>7</td>
<td>dB</td>
</tr>
<tr>
<td>Bandwidth efficiency ($K_{bw}$)</td>
<td>1</td>
<td>(bits/sec)/Hz</td>
</tr>
<tr>
<td>TX power amplifier efficiency ($\eta$)</td>
<td>50</td>
<td>%</td>
</tr>
<tr>
<td>Number of bits per packet ($N_b$)</td>
<td>100</td>
<td>-</td>
</tr>
<tr>
<td>Startup time ($t_s$)</td>
<td>250</td>
<td>$\mu$s</td>
</tr>
<tr>
<td>Fixed RX power ($P_{R_f}$)</td>
<td>0.5</td>
<td>mW</td>
</tr>
<tr>
<td>Fixed TX power ($P_{T_f}$)</td>
<td>0.5</td>
<td>mW</td>
</tr>
<tr>
<td>TRX baseband power per unit datarate ($P_B$)</td>
<td>0.1</td>
<td>mW/MHz</td>
</tr>
<tr>
<td>LNA noise-power constant ($K_L$)</td>
<td>1.52</td>
<td>mW</td>
</tr>
</tbody>
</table>

where $P_{TX}$ is fixed as the sensitivity is fixed in this case and assuming $F_R = F_L$. The ON times of the RX and the TX are assumed to be equal; supposing a perfectly synchronous system. To minimize the energy consumption, from (2.9) the following result is obtained:

$$\frac{dE_T}{dR} = 0 = \Rightarrow R_{opt} = K_{FD} \left( 1 + \sqrt{\frac{K_L}{P_{R_f} + P_{TX}}} \right)^{-1}$$  \hspace{1cm} (2.10)

As an example, if $K_{FD} = 10$ Mbps (20 dB NF for a datarate of 100 kbps and a sensitivity of -97 dBm) then $R_{opt} = 4.5$ Mbps by (2.10) and corresponding NF = 3.5 by (2.8). Clearly, the optimum data rate changes with $K_{FD}$ which changes with the RX sensitivity. Therefore this approach can be improved to minimize transceiver energy.

### 2.3.2 Data rate and noise figure specification for minimum energy duty-cycled radio communication

In this section, the transceiver datarate and RX NF are optimized together for a given application (link budget, operating frequency), architecture (SNR, TX efficiency), MAC protocol and technology. To minimize energy, the fixed RX sensitivity assumption in Section 2.3.1 needs to be removed. This helps to develop a combination of the two trade-offs discussed in Sections 2.2 and 2.3.1. In this case, (2.8) is not valid because the RX sensitivity is no longer fixed.

From (2.6), the energy consumed in the TRX to transfer one packet of $N_b$ bits can be
Chapter 2. Energy Minimization in Duty-cycled Radio Transceivers

modeled as:

\[ E_T = \frac{N_b}{R} \left( P_{RF} + P_{TF} + \frac{K_L}{F_R - 1} + \frac{SNR \cdot kT \cdot LB \cdot F_R \cdot R}{\eta K_{bw}} \right) \]  \hspace{1cm} (2.11)

The baseband power consumption, until now which was assumed to be incorporated in the fixed power in receiver and transmitter, changes with the datarate. The fixed power in (2.11), i.e. \((P_{RF} + P_{TF})\) has to be modified to take that into consideration. The RX and TX also need some startup time to be ready to operate. Again here a perfectly synchronous system is assumed which means both RX and TX are ON only for the required transmission time. In practice, the TX may initiate the communication and wait for the RX to turn ON for a considerable amount of time. Or the RX may turn ON periodically to check for any input signal. One of these cases will be addressed in the next section. The startup time is dominated by the startup time of a clock generator such as the phase lock-loop (PLL), and is typically similar in value for the RX and the TX [60]. Although the power consumption during startup can be less than the operating power consumption, for simple analysis, the startup power consumption is assumed to be the equal to the power during the operating time. Therefore, (2.11) can be modified accordingly:

\[ E_T = \left( \frac{N_b}{R} + t_S \right) \left[ P_F + R \cdot P_B + \frac{K_L}{(F_R - 1)} + \frac{SNR \cdot kT \cdot LB \cdot F_R \cdot R}{\eta K_{bw}} \right] \]  \hspace{1cm} (2.12)

where \(t_S\) is the RX/TX startup time in second, \(P_F\) is the total power consumption (watt) independent of the NF and datarate, \(P_B\) is the TRX baseband power consumption per unit baseband frequency (watt/Hz). The baseband frequency is assumed to be proportional to the datarate. Both the RX and TX part of the baseband power is incorporated in \(P_B\). Here other assumptions are: 1) The power consumption of the RX and the TX while in OFF-mode is negligible. 2) The data propagation time is negligible compared to the bit period. The data rate and noise figure have to just satisfy (2.12), there is no other limitation on the noise figure here. Let us consider a scenario corresponding to the values as listed in Table 2.2. The total energy consumption for the transmission of one packet of 100 bits as a function of datarate (\(R\)) and NF is plotted in Figure 2.3. It shows that indeed there is an datarate and NF value which results in minimum energy. For this given scenario, the optimum \(NF_{opt}\) is 8 dB and optimum datarate (\(R_{opt}\)) is 1.25 Mbps. Table 2.3 compares this result with two other energy optimization approaches. In the first case, the datarate is chosen at 100 kbps and NF is optimized by (2.7), i.e. the approach described in Section 2.2, and in the second case, the datarate is optimized by (2.10) for a NF of 3.5 dB, i.e. the approach described in Section 2.3.1. The transceiver energy calculated by (2.12) in both of those approaches are
2.3. Transceiver parameters for energy efficient duty cycled radio

Figure 2.3: Transceiver energy consumption (in nJ) to communicate $N_b = 100$ bits, shown as a function of RX noise figure and datarate; $E_{\text{min}}=569$ nJ with $NF_{\text{opt}}=8$ dB and $R_{\text{opt}}=1.25$ Mbps.

larger than the optimum obtained by the combined approach.

2.3.2.1 Boundary conditions of the energy minimization

There are some boundary conditions which have to be satisfied to make this method successful. Although the plot shows a wide range of datarate and NF values, not all of these combinations are acceptable in practice. The datarate has to be restricted to a range from the minimum datarate required by the application to a value which supports the available channel bandwidth and modulation scheme. The boundary of the NF is determined by the technology, RX circuit topology, design and chip area etc. The power consumption and NF trade-off approximated in (2.2) may change outside a range. Another factor is the battery efficiency which gets degraded for very high datarate as the instantaneous power is surged to a very high value, even if the overall energy is low. The requirement of an impractically larger capacitor [61] limits the acceptable maximum instantaneous power consumption and hence restricts the maximum achievable datarate.
Table 2.3: Energy consumption to communicate $N_b = 100$ bits; Comparison of three approaches of TRX system optimization

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Optimized NF (Section 2.3.1)</th>
<th>Optimized datarate (Section 2.2)</th>
<th>Proposed NF-datarate optimized (Section 2.3.2)</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data rate</td>
<td>100 kbps</td>
<td>4.5 Mbps</td>
<td>1.2 Mbps</td>
<td>bps</td>
</tr>
<tr>
<td>NF</td>
<td>14 dB</td>
<td>3.5 dB</td>
<td>8 dB</td>
<td>dBm</td>
</tr>
<tr>
<td>TX power</td>
<td>-13 dBm</td>
<td>-7 dBm</td>
<td>-8 dBm</td>
<td>dBm</td>
</tr>
<tr>
<td>RX Sensitivity</td>
<td>-103 dBm</td>
<td>-97 dBm</td>
<td>-98 dBm</td>
<td>dBm</td>
</tr>
<tr>
<td>Transceiver Energy</td>
<td>1466 nJ</td>
<td>837 nJ</td>
<td>569 nJ</td>
<td>nJ</td>
</tr>
</tbody>
</table>

2.4 Transceiver parameters for minimum energy wakeup radio (WuRx) for a slot based MAC protocol

A wakeup radio RX architecture consists of an extra RX (called the wakeup-receiver) to wakeup the main RX when required [30]. The overall energy consumption can be reduced assuming an ultra low power wakeup receiver (WuRX) is available [32]. It is clear that the ON time for this WuRX is different to the main RX. Therefore, the minimum energy datarate and NF for the WuRX is distinct to the main RX. In fact this is the most effective way in which wakeup radio power consumption can be reduced compared to the main RX. Otherwise both RX might consume similar power as they have to achieve the same link budget and robustness. For a slot-based MAC protocol proposed for a WuRX [62], this optimization method is applied.

In [62], the WuRX is also duty cycled and turned ON periodically to sense the channel. The main RX is only ON for the time required to receive the data. To synchronize the clocks of the sensor nodes, a “sync beacon” signal is sent periodically (called beacon period) to correct the clock error among the sensor nodes. If the clock edge error is a $\pm e_{clk}$ fraction of the clock period, the maximum time uncertainty of a clock phase between the TX and the RX is $2(e_{clk}/R_B)$, where beacon rate = $R_B$. The wakeup radio has to operate for this extra time so that the error can be tolerated. The total energy consumption in ‘wakeup’ is the addition of the energy consumed in the WuRX and the energy consumed in the TX sending the wakeup bits. Total ON time of the receiver is $4e_{clk}/R_B + N_W/R_W + t_{SW}$ and for the transmitter is $N_W/R_W + t_{SW}$ where subscript $W$ specifies the parameters for wakeup radio, $t_{SW}$ is the wakeup radio startup time, $R_W$ is the datarate of the wakeup radio, and $N_W$ is the number of bits required to transmit to wakeup the main radio RX. The link budget of the wakeup receiver needs to be equal or greater than the main receiver so that communication can happen over a distance supported by both main RX and WuRX. The SNR requirement is assumed to
2.4. Transceiver parameters for minimum energy wakeup radio (WuRx) for a slot based MAC protocol

be equal to the main receiver. Assuming a similar front end structure, $K_L$ also remains the same for WuRX. With these assumptions, the total energy consumed in one second due to the wakeup RX and TX can be obtained by modifying (2.12) accordingly as:

$$E_{T1} = (R_B + R_{PW}) \left\{ \left( \frac{4e_{clk}}{R_B} + \frac{N_W}{R_W} + t_{SW} \right) \left[ P_{Rf} + R_W P_{WB} + \frac{K_L}{(F_W - 1)} \right] \right. + \left. \left( \frac{N_W}{R_W} + t_{SW} \right) \left[ P_{Tf} + R_W P_{WB} + \frac{SNR kT LB F_W R_W}{\eta K_{bw}} \right] \right\}$$

(2.13)

where $F_W$ is the noise factor of the wakeup radio, and $P_{WB}$ and $P_{WB}$ are the baseband power constant (power per unit baseband frequency) of the WuRX and the TX respectively. The wakeup receiver is switched ON for both clock correction (at beacon rate, $R_B$) and to receive wakeup bits (at packet rate, $R_{PW}$). The energy consumption is dependent on the relative ratio between the packet rate and the beacon rate. To take that into account, (2.13) is multiplied by $(R_B + R_{PW})$ to obtain the average energy consumption in one second ($E_{T1}$). One second is used as the unit time so that it can also indicate the average power consumption of the TRX.

Equation (2.13) is used to deduce the NF and datarate for minimum energy for the specifications/parameters listed in Table 2.4. Table 2.5 shows the average wakeup energy ($E_{T1}$) at the optimum datarate and NF for three different clock inaccuracies. Table 2.5 also shows the optimum beacon rates corresponding to those clock inaccuracies, taken from [62]. The optimum value of the datarate and noise factor is dependent on the clock accuracy. The energy associated with the sync clock generation is assumed to be fixed for simplicity. The TRX energy consumption as a function of datarate and NF is plotted in Figure 2.4 for a clock accuracy of 100 ppm. Other specifications and constants are the same as in Table 2.2. The optimum datarate is lower and the NF for minimum energy is higher than that in Section 2.3.2. Both of these choices lead to less RX power and more TX power. As the WuRX is ON for a longer time, it is expected to obtain an optimum with worse RX sensitivity to minimize RX power. This way, despite having the same link budget and architecture (as both targeted to be ultra low power), the WuRX power consumption can be lower than the main receiver; supporting the basic WuRX assumption.

### 2.4.1 Discussion

A different optimum datarate in the WuRX and the main RX minimizes the overall energy consumption. However, there are some consequences using different datarate and NF for those two RXs. At the wakeup of the main RX, the TX has to switch from transmitting
Table 2.4: List of design specifications of Wakeup radio

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandwidth efficiency ($K_{bw}$)</td>
<td>1</td>
<td>(bits/sec)/Hz</td>
</tr>
<tr>
<td>Link budget ($LB$)</td>
<td>90</td>
<td>dB</td>
</tr>
<tr>
<td>Signal to noise ratio ($SNR$)</td>
<td>7</td>
<td>dB</td>
</tr>
<tr>
<td>LNA noise-power constant ($K_L$)</td>
<td>1.52</td>
<td>mW</td>
</tr>
<tr>
<td>Wakeup radio packet rate ($R_{PW}$)</td>
<td>1</td>
<td>/minute</td>
</tr>
<tr>
<td>Number of wakeup bits ($N_W$)</td>
<td>100</td>
<td>-</td>
</tr>
<tr>
<td>Wakeup radio startup time ($t_{SW}$)</td>
<td>250</td>
<td>µs</td>
</tr>
<tr>
<td>Wakeup radio fixed RX power ($P_{RF}$)</td>
<td>0.25</td>
<td>mW</td>
</tr>
<tr>
<td>Wakeup radio fixed TX power ($P_{TF}$)</td>
<td>0.25</td>
<td>mW</td>
</tr>
<tr>
<td>Wakeup RX/TX baseband power per unit datarate ($P_{W Br}/P_{W Bt}$)</td>
<td>10</td>
<td>µW/MHz</td>
</tr>
</tbody>
</table>

Table 2.5: Minimum energy of wakeup TRX for three different clock accuracies

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Case1</th>
<th>Case2</th>
<th>Case3</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock accuracy ($e_{clk}$)</td>
<td>10000</td>
<td>1000</td>
<td>100</td>
<td>ppm</td>
</tr>
<tr>
<td>Beacon rate ($R_B$)</td>
<td>0.2</td>
<td>0.09</td>
<td>0.03</td>
<td>Hz</td>
</tr>
<tr>
<td>Optimum wakeup RX NF</td>
<td>24</td>
<td>20</td>
<td>18</td>
<td>dB</td>
</tr>
<tr>
<td>Optimum wakeup datarate</td>
<td>100</td>
<td>175</td>
<td>250</td>
<td>kbps</td>
</tr>
<tr>
<td>TX output power</td>
<td>-2.8</td>
<td>-4.4</td>
<td>-4.8</td>
<td>dBm</td>
</tr>
<tr>
<td>Average wakeup energy in one second ($E_{T1}$)</td>
<td>11560</td>
<td>1375</td>
<td>208</td>
<td>nJ</td>
</tr>
</tbody>
</table>

wakeup bits at one datarate to data bits at a different datarate. At the time when the main RX is switching ON, because of low datarate of the WuRX, it may switch ON the main RX at an incorrect time instant. The time error can be as large as the WuRX bit period. For correct operation, the WuRX has to switch ON the main RX at least one wakeup bit period before receiving the actual data; to guarantee that the main radio wakes up before actual data is reached. The TX power has to be changed from wakeup bit to actual data transmission.

The approach presented here can also be extended to a mixer first radio as it can be shown that a passive mixer has a noise-power tradeoff property similar to (2.2) with a different value of $K_L$ (Appendix A.1). In Appendix A.2, it is shown that the same power-noise tradeoff property also holds for two cascaded blocks controlling the receiver front end noise figure. Therefore for either 'LNA + mixer' or 'mixer + IF amplifier' front-end, noise-power can be related by (2.2) just by changing the constant $K_L$. 
2.5 Discussion and Summary

In this section, the energy minimization proposed in Section 2.3.2 is applied to a short range, low power WSN. Starting from the communication distance, the free space path loss can be calculated by the following equation:

$$L_{FS} = 20 \cdot \log_{10} \left( \frac{4\pi f_{RF}d}{c} \right)$$  \hspace{1cm} (2.14)

where $d$ is the distance between the TX and RX, $f_{RF}$ is the RF signal frequency and $c$ is the speed of light in vacuum. For a distance, $d = 5 \, m$ and $f_{RF} = 2.45 \, GHz$, the free space path loss is 54 dB. Having some margin for fading etc., the target link budget chosen for communication is 60 dB. Table 2.6 lists the design specifications modified from Table 2.2 for a more suitable short range and ultra low power application. The SNR requirement for low power communications is usually relaxed, so we choose SNR=12 dB. Also, the fixed power in RX and TX is reduced. Because of the availability of non-PLL and fast starting TRX, the startup time also reduced. For very low duty cycled systems the TRX power consumption at switched OFF mode, say $P_{OFF}$ can also have a significant effect, so it is considered here. Using (2.12), the energy consumed to transfer $N_b$ bits (assuming one.
packet per second) in the TRX can be represented as:

\[
E_T = \left( \frac{N_b}{R} + t_S \right) \left[ P_F + R_P + \frac{K_{RX}}{(F_R - F_{\text{min}})} + \frac{\text{SNR} \cdot kT \cdot LB \cdot F_R \cdot R}{\eta \cdot K_{bw}} \right] + \left[ 1 - \left( \frac{N_b}{R} + t_S \right) \right] P_{\text{OFF}} \tag{2.15}
\]

where \( F_{\text{min}} \) is minimum noise factor for the receiver, \( K_{RX} \) is the RX noise power constant, \( F_R \) is the RX noise factor and \( P_{\text{OFF}} \) is the OFF mode power consumption of the TRX. The ON time is assumed to be less than one second in (2.15). Using the values listed in Table 2.6, the optimum value of NF is 18 dB and datarate is 11 Mbps. Although in Appendix A it is shown that \( F_{\text{min}} \) can be assumed to be one for ultra-low power designs, in this section \( F_{\text{min}} \) is taken as 2.5 from the passive mixer simulation results (Appendix A) for more accurate optimum calculations.

The influence on minimum energy NF, datarate and energy per bit (\( E_T/N_b \)) due to various parameter changes are plotted in Figure 2.5. The default specifications in Table 2.6 are used in equation (2.15) to find the noise figure/datarate combinations with the lowest energy per bit. Figure 2.5a shows that with the increase of \( K_{RX} \), \( NF_{\text{opt}} \) increases as well as the optimal datarate. This is expected because higher \( K_{RX} \) means higher cost (power) for receiver noise figure. High \( K_{RX} \) could be either due to receiver front end architecture and circuit choice or due to tougher performance requirement apart from NF or power consumption (such as linearity). In those cases relaxing the NF target for the receiver tends to reduce TRX energy consumption.

Figure 2.5b shows the change of \( NF_{\text{opt}} \) and \( R_{\text{opt}} \) as a function of LB. \( NF_{\text{opt}} \) reduces with the increase of LB because a higher LB puts more burden to the TX and thus increasing power in RX to reduce NF is better for TRX energy. The change of \( R_{\text{opt}} \) is more complicated as indicated by the non-monotonous nature of the curve. When LB is very low, the transmitter power can be ignored compared to the fixed power and a high \( NF_{\text{opt}} \) makes sure that the RX front-end power is also negligible. Therefore, the optimum condition is determined by the first two terms of the operating power in (2.15). Ignoring the last two terms, the \( R_{\text{opt}} \) can be obtained as:

\[
R_{\text{opt}} = \sqrt{\frac{N_b P_F}{t_S P_B}} \tag{2.16}
\]

With the values in the Table 2.6, the \( R_{\text{opt}} \) calculated as 7 Mbps, which corresponds with Figure 2.5b at very low LB. At around 50 dB, the \( R_{\text{opt}} \) starts to increase. This is because with LB, as the energy of the TX and the RX fronted increases, it makes sense to increase
Table 2.6: List of design specification in scenario-II; Targeted to a low power short-range communication system.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>RF Frequency (ISM band) ($f_{RF}$)</td>
<td>2.45</td>
<td>GHz</td>
</tr>
<tr>
<td>Communication distance ($d$)</td>
<td>5</td>
<td>m</td>
</tr>
<tr>
<td>Link budget ($LB$)</td>
<td>60</td>
<td>dB</td>
</tr>
<tr>
<td>Signal to noise ratio ($SNR$)</td>
<td>12</td>
<td>dB</td>
</tr>
<tr>
<td>Bandwidth efficiency ($K_{bw}$)</td>
<td>1</td>
<td>(bits/sec)/Hz</td>
</tr>
<tr>
<td>Number of bits in one second (/per packet) ($N_b$)</td>
<td>1000</td>
<td>-</td>
</tr>
<tr>
<td>Startup time ($t_s$)</td>
<td>50</td>
<td>$\mu$s</td>
</tr>
<tr>
<td>RX noise-power constant ($K_{RX}$)</td>
<td>2.5</td>
<td>mW</td>
</tr>
<tr>
<td>Fixed RX or TX power ($P_F$)</td>
<td>0.05</td>
<td>mW</td>
</tr>
<tr>
<td>Minimum RX noise factor ($F_{min}$)</td>
<td>2.5</td>
<td>-</td>
</tr>
<tr>
<td>modulator/demodulator power per datarate ($P_B$)</td>
<td>20</td>
<td>$\mu$W/MHz</td>
</tr>
<tr>
<td>RX/TX sleep current ($P_{OFF}$)</td>
<td>500</td>
<td>nW</td>
</tr>
</tbody>
</table>

datarate so that the TRX can be switched off quickly to save energy. After some more increase of LB however, the TX power increases so much that decreasing data rate helps to reduce more TX power then the ON time reduction, because the NF reduction costs too much power at around or below 3 dB. Figure 2.5c shows that with increasing number of bits the $R_{opt}$ increases sharply and $NF_{opt}$ reduces. Such increase of $R_{opt}$ is because of the assumption of a fully synchronized mechanism to duty-cycle the TRX. In a more practical case, if the required extra ON time of the RX due to clock inaccuracy is added in the model, this effect will reduce. Figure 2.5d shows that with increasing $t_s$, $NF_{opt}$ goes high and $R_{opt}$ decreases. Please note that the effect of link budget change as shown in Figure 2.5b can also predict the effect of changed SNR requirement or changed achievable TX power amplifier efficiency according to (2.15). For example the effect of 3 dB higher link-budget is same as increasing required SNR by 3 dB or decreasing TX power amplifier efficiency by two times.

### 2.5.1 Conclusion

To minimize the energy consumption of a wireless sensor network transceiver, a method of choosing the optimum RX noise figure and datarate is described. It is shown that there is an optimum combination of NF and datarate which minimizes the overall transceiver energy. Rather than choosing a predefined value from intuition, this approach can lead to a significant reduction of the energy consumption for a given application, MAC protocol and
receiver architecture. This method can also be applied to a wakeup receiver architecture to reduce wakeup energy. It shows an effective way to reduce the WuRX power consumption compared to the main receiver.
Chapter 3

Phase-accurate Quadrature Frequency Divider for Low Power Transceivers

3.1 Introduction

As discussed in Chapter 1, interference robustness is an important property for WSN and other wireless transceivers. Therefore, high image rejection and harmonic rejection are necessary, and for these low-phase-error multi-phase clock generation (MPCG) is essential [63] [64]. Quadrature generating dividers are often used to generate quadrature clocks in I-Q receivers and higher number of phases are used in harmonic reject mixer [65]. Because of high frequency operation, the power consumption of these dividers is often a significant portion of the total receiver power in low power applications. Therefore selecting a divider for best phase error and power consumption is essential for low power and interference robust receivers. In this chapter, two commonly used multiphase generating dividers are compared to improve the combined performance of phase-error and power consumption. This chapter is entirely same as [47], except some minor text changes in the introduction.

Phase errors originate from delay deviations in MPCG blocks, e.g. delay elements in a delay locked loop or Flip-Flops (FF) in a shift-register or divider based MPCG [66]. Delay deviation can originate from the intrinsic properties (mismatch, noise) of the FF in a divider itself, or be caused by external influences like supply noise. To reduce the effect of supply noise, CML logic is often used. However, if the power supply noise can be adequately reduced by regulation and decoupling capacitors, the question is which type of FF offers the lowest jitter for a given amount of power. At the International Solid-State Circuits Conference increasingly Dynamic Transmission Gate Logic (DTGL) and standard CMOS logic dividers are being used in PLLs and other jitter critical applications (e.g. refs
Chapter 3. Phase-accurate Quadrature Frequency Divider for Low Power Transceivers

[65, 67]). Good achieved results make it plausible that the supply decoupling problem can be solved to a sufficient degree. Among the intrinsic error sources, the timing errors due to mismatch are much larger than from device noise [68]. As mismatch is static, it adds a skew to a one-phase clock. However, if multiple clock phases contribute to one output at different moments in time, deterministic “mismatch jitter” results [66, 69]. The mismatch-jitter term used in this chapter is defined as the random fluctuation of the delay due to device mismatch between any two output (could be differential) phases from MPCG. Although mismatch-jitter can be reduced by digital calibration, this adds considerable cost and complexity. As discussed in [66, 70], putting identical circuits in parallel (W-scaling, admittance/impedance scaling) reduces mismatch jitter at the cost of higher area and power consumption. Therefore, just comparing mismatch-jitter without considering power will give a highly sizing dependent result. Hence, we normalize jitter-variance to power consumption, as in [66] and use the Jitter-Power Figure of Merit (FoM):

\[ \text{FoM} = \sigma_{tm}^2 P_d \]  \hspace{1cm} (3.1)

where \( \sigma_{tm} \) is the timing variance due to mismatch and \( P_d \) is the power dissipation. This FoM has a fundamental basis and allows for comparing differently sized circuits fairly, similar to normalizing oscillator phase noise or filter SNR to Power. In [65], DTG-FFs were used and able to achieve very low phase errors at much lower power consumption than CML. Explorative simulations in [70] confirmed that DTG-FFs have significant advantages over CML-FFs for MPCG. However, we would like to understand under which conditions (frequency, number of phases) this is true and how technology affects the conclusions. Although the speed, power and power-delay has been analyzed fundamentally extensively for several FF topologies (e.g. [71, 72]), there is not much work to optimize Jitter-Power performance. This chapter hence derives analytical equations to estimate Jitter, Power and FoM for both DTG and CML-FFs. Such analytical equations are valuable for insight, to guide the initial design of FFs.

3.2 Flip-flop power and mismatch jitter modeling

We model the mismatch jitter and power consumption, for an N-phase MPCG/divider implemented using DTG-FFs and CML-FFs as depicted in Figure 3.1 and 3.3 for the case \( N = 4 \). The differential divider outputs (e.g. pair I+, I-) will be analyzed, so that a fair comparison can be made with a CML-FF which has a differential output. To provide insight, we keep the equations simple and use first order device equations rather than the
more complicated short channel models. Evaluating (3.1) for a MPCG with N DTG-FFs we find:

![Diagram of MPCG using DTG-FFs (N=4)](image)

Figure 3.1: MPCG using DTG-FFs (N=4)

![Diagram of one DTG-FF](image)

Figure 3.2: One DTG-FF

\[
FoM_{DTG} = \frac{\sigma^2_{DTG-FF}(NP_{DTG-FF} + P_{DTG-INBUF})}{N}
\]

(3.2)

where \(\sigma^2_{DTG-FF}\) is the mismatch-jitter variance at the differential output of the divider (variation in FF differential delay) and N is the number of phases.

\(P_{DTG-FF}\) and \(P_{DTG-INBUF}\) are power consumptions of a single FF and all input clock buffers (two inverters in this case) respectively. As we aim for insight in FF design (used in a MPCG), we chose to analyze ‘FoM per flip-flop’. Thus we divide (3.2) by N to find a FF FoM, assuming all FFs are identical and contribute the same mismatch jitter:

\[
FoM_{DTG-FF} = \frac{FoM_{DTG-MPCG}}{N} = \frac{\sigma^2_{DTG-FF}(P_{DTG-FF} + P_{DTG-INBUF})}{N}
\]

(3.3)

For a MPCG with CML-FFs as in Figure 3.3, however, only N/2 FFs are required because
Figure 3.3: MPCG with CML-FFs for N=4 (top), CML flipflop and CML latch (bottom)

differential outputs are already available. Thus its expression of FoM per FF is obtained by dividing FoM of MPCG by N/2 as follows:

\[ \text{FoM}_{\text{CML-FF}} = \frac{\text{FoM}_{\text{CML-MPCG}}}{N/2} = \sigma_{\text{CML-FF}}^2 (P_{\text{CML-FF}} + \frac{2P_{\text{CML-INBUF}}}{N}) \]  

(3.4)

where \( P_{\text{CML-FF}} \) and \( P_{\text{CML-INBUF}} \) are power consumptions of a single FF and the input clock buffer respectively. We assumed that the presence of start-up initialization switches can be neglected, and that all FFs are triggered by the same edge (positive edge of CLK+ - CLK-) of a shared differential clock. Thus a deterministic time shift in that clock edge is common for all the FFs and does not contribute to phase errors between clock phases. So, even if a large number of cascaded buffers is used in front of a FF to drive N big FFs, buffer timing errors fall out and the phase error is dominated by the FF. In contrast, if buffers are added after the FF, both the FF and the buffer contribute mismatch errors. To minimize total mismatch...
3.2. Flip-flop power and mismatch jitter modeling

Figure 3.4: Clock input to the output delay path of a DTG-FF

jitter, buffers should be added before the FF in case it has to drive a large capacitive load. As such buffers are generally scaled up (“tapered buffer chain”), the overall power consumption is dominated by the FFs and the last buffer preceding the FF, justifying just one clock buffer stage in the FoM model. In a master-slave D-FF the slave-latch drives the load and thus its delay variation renders mismatch-jitter. To improve FoM, the master-latch can be scaled down compared to the slave-latch. As this is possible for both logic families, for simplicity we keep the master and slave latch identical. We derive FoM equations for DTG-FFs in sub-section 3.2.1 and for CML-FFs in sub-section 3.2.2.

3.2.1 FoM of a Dynamic Transmission Gate Flip-Flop

The mismatch-jitter of a DTG-FF (Figure 3.2) is the variation of clock-to-output delay. The critical delay path is drawn in Figure 3.4. First we model the transmission gate delay modeled by its equivalent RC-time constant [73]. Here we take a simplified first order TG delay where the equivalent resistance is assumed to be constant over the transition range (Figure 6.48 in [74]). Using the simple square-law MOS transistor model, the equivalent TG resistance can be obtained. From the TG equivalent resistance, the delay from the 50% input level to the 50% output level can be written as:

\[ t_{TG} = \frac{2(\ln(2))V_{DD}(C_L + C_{int})}{K_n(V_{DD} - V_{Tn})^2 + K_p(V_{DD} - |V_{Tp}|)^2} \]  

(3.5)
where $C_L$ is the output capacitance, $K = \mu C_{ox}W/L$, $V_T$ is the threshold voltage, while suffixes $n$ and $p$ refer to nMOS and pMOS transistors respectively. Equation (3.5) is valid for both high-to-low (H-L) and low-to-high (L-H) transitions. We modify the equivalent resistance by adding the driving inverter resistance (see Figure 3.4) to estimate the delay better. For a L-H output transition, the pMOS in the inverter is active and operates in the triode region. The same is true for the nMOS for a H-L transition. Adding these resistances, the delay for the differential (anti-phase) output, which is the average of an H-L and L-H delay, can be written as:

$$t_{TG,f_{AVG}} = \frac{\ln(2) \cdot (C_L + C_{int})}{2V_{DD}} \left[ \frac{1}{K_n(V_{DD} - V_Tn)^2 + K_p(V_{DD} - |V_{TP}|)^2} + \frac{1}{2K_n(V_{DD} - V_Tn)} + \frac{1}{2K_p(V_{DD} - |V_{TP}|)} \right]$$

(3.6)

where $C_{int}$ is the load capacitance due to the transmission gate itself. The last two resistance terms in (3.6) model inverter triode resistances for equally sized inverter and TG transistors. In practice also:

$$V_{Tn} \approx |V_{TP}| \text{ and } K_n \approx K_p$$

(3.7)

Using (3.7) and defining the ratios below, (3.6) can be written as:

$$t_{TG,f_{AVG}} = \frac{(\ln(2))L^2(\gamma_c + r_l + 0.5)(1 + r_\mu)(2V_{DD} - V_{TN})}{\mu(V_{DD} - V_{TN})^2}$$

(3.8)
3.2. Flip-flop power and mismatch jitter modeling

where \( r_l \) is the loading ratio of a FF, i.e., its \( C_L \) expressed in terms of its input capacitance, ratio \( r_\mu \) is the pMOS to nMOS width-ratio \((W_p \div W_n, \text{typically } 2.5, \text{equal to the electron-to-hole } \mu\text{-ratio})\), \( \mu \) is the mobility of an nMOS transistor, \( \gamma_c \) is the ratio of drain to gate capacitance of a MOS transistor (bias independent for simplicity). Although the delay equation (3.8) neglects the effect of finite rise/fall time, it gives a reasonable estimate (see Figure 3.5). Mismatch jitter is now obtained taking partial derivatives of (3.6) to take care of the nMOS and pMOS mismatch difference due to different area. Applying approximation (3.7) and after some algebra we can obtain the mismatch-jitter variance:

\[
\sigma_{DTG-FF}^2 = \frac{(\ln(2))^2 V_{DD}^2 L^4 \gamma_c + r_l + 0.5)^2}{4 \mu^2 r_\mu (1 + r_\mu)^{-3} (V_{OD})^4} \cdot \left[ (1 + d_o^2) \frac{\sigma_{K_n}^2}{K_n^2} + \frac{(4 + d_o^2) \sigma_{V_{Tn}}^2}{(V_{OD})^2} \right]
\] (3.9)

Here \( \sigma_{V_{Tn}} \) and \( \sigma_{K_n} \) are the standard deviation of \( V_{Tn} \) and \( K_n \) mismatch respectively, assumed to be the same for a pMOS. The overdrive \( V_{OD} = (V_{DD} - V_{Tn}) \) and \( d_o \) is the normalized overdrive ratio of \( V_{OD} \) w.r.t. \( V_{DD} \). As the total load device size at the output node is bigger than the device sizes inside the flipflop, its capacitive mismatch is less important than \( K \) mismatch and it is neglected. When used inside an MPCG, each FF’s output drives another FF along with the external load. To take this into consideration, we replaced \( r_l \) by \((r_l + 1)\) in (3.9). The power consumption of a CMOS inverter can be approximated in terms of its nMOS gate capacitance, \( C_{gn} \) as,

\[
P_{INV} = f_O V_{DD}^2 C_{gn} (1 + r_\mu) (\gamma_c + r_l)
\] (3.10)

where \( f_O \) is the output clock frequency. This assumes that the dynamic charging/discharging power is dominant over short-circuit-power and leakage power. The dynamic power consumption of a DTG-FF (Figure 3.2), can be expressed as:

\[
P_{DTG-FF} = f_O V_{DD}^2 C_{gn} (1 + r_\mu) (2(3 \gamma_c + 1) + r_l)
\] (3.11)

And the input buffer power consumption per FF is:

\[
P_{DTG-FF} = 2 f_O V_{DD}^2 C_{gn} (1 + r_\mu) N
\] (3.12)
where the input clock frequency, \( f_i \) is expresses as \( N f_o \). With the help of (3.1), (3.3), (3.9) and (3.12), and some algebra we get:

\[
\text{FoM}_{DTG-FF} = \frac{f_o V_{DD}^4 L^4 C_{OX}}{\mu^2 (V_{OD})^4} F_{DTG}(r_l) \cdot \left[ (1 + d_o^2) A_{Kn}^2 + \frac{(4 + d_o^2) A_{V_{Tn}}^2}{(V_{OD})^2} \right]
\]  

(3.13)

where \( A_{V_{Tn}} \) and \( A_{Kn} \) are the technology dependent mismatch constants and \( F_{DTG}(r_l) \) is a function which depends on the circuit topology used in the DTG-FF. For Figure 3.2 it is:

\[
F_{DTG}(r_l) = \frac{(2(3\gamma + 1 + N) + r_l)(\gamma + r_l + 1.5)^2}{4ln(2)^2 r\mu (1 + r\mu)^{-4}}
\]  

(3.14)

Here we approximate the MOS gate capacitance as \( C_{OX} \cdot W \cdot L \). As the FoM is by its definition independent of admittance scaling, it only makes sense to optimize the FoM of the FF by changing width-ratios such as \( r\mu \) and \( r_l \). We used \( r\mu = 2.5 \) to match the rise and fall delays of the FF. The clock-buffer size is chosen to be close to its optimum 2.5 [75] for minimum power and mismatch-jitter product.

To optimize FoM, we see that lowering \( V_{DD} \) is very effective, while short channels (small \( L \)) are also very beneficial. When \( N \) is increased, the FoM increases via \( F_{DTG} \) according to (3.13) assuming \( f_o \) is constant. This is expected since for constant \( f_o \) and higher \( N \), \( f_i \) goes up, increasing dynamic power proportionally, whereas mismatch jitter remains the same according to (3.9). However, if we keep the \( f_i \) constant and increase \( N \), \( f_o \) will decrease and thereby decrease the dynamic power and hence the FoM.

### 3.2.2 FoM of a Current Mode Logic Flip-Flop (CML-FF)

The CML-FF in Figure 3.3 (top) consists of two identical CML master-slave latches. The delay variation of a CML-FF, added which is the same as that of a CML latch (Figure 3.3, bottom) is derived in analogy to that of a CML buffer as in [66]. For cascaded CML buffers the output load capacitance is normally dominated by the input transistors of the next CML stage. To minimize the load capacitance for the previous stage, the width of the nMOS has to be just enough to completely flip the bias current from one load resistor \( R_b \) to the other, see CML buffer in Figure 3.3, bottom. In that case, input transistor overdrive voltage is the same as the voltage swing \( V_S \) when the input is fully switched. Thus the bias current of a CML buffer (\( I_B \)) or a CML latch (\( I_L \)) in a CML-FF can be related to its voltage swing (\( V_S \))
3.2. Flip-flop power and mismatch jitter modeling

as:

\[ I_B = \mu C_{\text{OX}} \frac{W_B}{2L} V_S^2, \quad I_L = \mu C_{\text{OX}} \frac{W_L}{2L} V_S^2 \]  

(3.15)

where \( W_B \) and \( W_L \) are the widths of the input transistor of the buffer and the latch respectively. Using (3.15), the mismatch jitter of the FF given in [66] can be re-written as:

\[ \sigma_{\text{CML-FF}}^2 = I_{\text{CML}}^2 \left[ \frac{\sigma_{\delta C_L}^2}{C_L^2} + \frac{\sigma_{\delta R}^2}{R^2} + \frac{1}{((L/2) \cdot V_S)^2} \left\{ \frac{\sigma_{\delta V_{\text{Tn}}}^2}{4} + \frac{\sigma_{\delta R}^2}{K_n^2} + \frac{\sigma_{\delta R}^2}{R^2} \right\} \right] \]  

(3.16)

As power consumption of a CML buffer is \( V_{\text{DD}} I_B \), we obtain the CML buffer FoM from (3.16) in terms of basic technology, design and mismatch parameters as:

\[ \text{FoM}_{\text{CML-INBUF}} = \frac{V_{\text{DD}} C_{\text{OX}} L^2 (\gamma_c + r_l)^2}{2 \mu} \cdot \left[ \frac{4A_{\text{Tn}}^2}{V_S^2} + A_{K_n}^2 + \frac{3A_R^2}{r_{RM}} \right] \]  

(3.17)

where \( r_{RM} \) is the ratio of resistor and the input nMOS device area and \( A_R \) is a resistor mismatch constant. Here we ignore load capacitance mismatch (see Section 3.2.1) for simplicity. The load capacitance is modeled via load ratio \( r_l \).

To get the CML-FF FoM used in an MPCG, we need to know the relation between \( I_L \) and \( I_B \). The ratio of \( I_L \) and \( I_B \) is designed such that both buffer and FF have the same output slew-rate. This is to have an equal distribution of mismatch-jitter among cascaded stages. The clock buffer drives \( N/2 \) CML-FFs or \( N \) CML latches and the latch drives \((r_l + 2 + \gamma_c)\) times its total input-capacitance. Thus the buffer and CML-FF input transistor width ratio (also current ratio) is:

\[ \frac{I_B}{I_L} = \frac{W_B}{W_L} = \frac{N}{r_l + 2 + \gamma_c} \]  

(3.18)

Hence, the total power consumption per FF is:

\[ P_{\text{CML-FF}} + \frac{2P_{\text{CML-INBUF}}}{N} = (2I_L + \frac{2I_B}{N})V_{\text{DD}}. \]  

(3.19)

Changing (3.17) according to the load condition of a CML-FF in a MPCG and using (3.4) and (3.19) we obtain:

\[ \text{FoM}_{\text{CML-FF}} = \frac{V_{\text{DD}} C_{\text{OX}} L^2}{\mu} \cdot F_{\text{CML}}(r_l) \cdot \left[ \frac{4A_{\text{Tn}}^2}{V_S^2} + A_{K_n}^2 + \frac{3A_R^2}{r_{RM}} \right] \]  

(3.20)
where $F_{CML}$ is a function of $r_l$ specific to CML MPCG:

$$F_{CML}(r_l) = \frac{(r_l + 4\gamma_c + 3)}{(r_l + 4\gamma_c + 2)}(r_l + 2\gamma_c + 2)^2 \tag{3.21}$$

Two design choices can improve the FoM in (3.20): increasing the voltage swing (reduces $V_T$ mismatch effect), and reducing the load ratio (reduces the load capacitance and delay). We simulated with 1.2 V of power supply in a 90 nm CMOS technology and used 0.4 V of voltage swing which keeps all transistors more or less in saturation. The load ratio affects FF-delay and the mismatch-jitter variance in a similar manner, so that FoM and delay are proportional to each other when $V_{DD}$ and $V_S$ is fixed. Thus low delay is preferred as in [66].

Table 3.1: Parameters for jitter-power estimation in a 90 nm CMOS process

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Value</th>
<th>Parameters</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_O$</td>
<td>1 GHz</td>
<td>$\gamma_c$</td>
<td>0.5</td>
</tr>
<tr>
<td>$V_{Tn} = V_{Tp}$</td>
<td>350 mV</td>
<td>$\mu$ (nMOS)</td>
<td>8.5E-5 $m^2/Vs$</td>
</tr>
<tr>
<td>$C_{OX}$</td>
<td>18 fF/$\mu m^2$</td>
<td>$r_{\mu}$</td>
<td>2.5</td>
</tr>
<tr>
<td>$L$ (effective)</td>
<td>75 nm</td>
<td>$A_{Vt}$</td>
<td>3.7 mV.$\mu m$</td>
</tr>
<tr>
<td>$V_S$</td>
<td>400 mV</td>
<td>$A_K$</td>
<td>1%.$\mu m$</td>
</tr>
<tr>
<td>$r_{RM}$</td>
<td>4.6</td>
<td>$A_R$ (n+ poly)</td>
<td>1.4%.$\mu m$</td>
</tr>
</tbody>
</table>

To compare model with simulation, we calculated the power, mismatch-jitter and FoM using the values in Table 3.1 for a 90 nm CMOS process. We simulated 4-phase MPCGs.
for an input frequency $f_i = 4 \text{ GHz}$ and slew-rate of 48 V/ns. The DTG-FF nMOS width is $16 \mu m$ (minimum length given by the technology is used) and the CML-FF ($R = 67 \text{ ohm}, I_L = 6 \text{ mA}$) input device is $55 \mu m$ so that the input capacitance considering ratio $r_{\mu}$ is equal for both FFs. For mismatch jitter, we did Monte Carlo simulations with 100 iterations for ‘only mismatch’ variations. The power consumption ($P_d$) and the mismatch-jitter (Mj) model results are compared with simulation results in Figure 3.6a and Figure 3.6b respectively with changing load ratio $r_l$, i.e. changing load capacitance. The power consumption has some deviation from the model due to the square-law-model inaccuracy. Simulated DTG-FF Mj is less than modeled, as we assumed equal $A_{VT}$ for the pMOS and nMOS (actually pMOS mismatch is less). In contrast, simulated CML-FF Mj is more than modeled due to the approximated first order delay equation used. We accept these model errors to keep model equations simple. The simulated delay, power, Mj and FoM are shown in Table 3.2 for $r_l=1$ for both FFs. A column for $r_l = 1/8$ is added for DTG to show that DTG power consumption can be even higher than CML depending on the sizing, where device width is increased keeping the load capacitance the same. It demonstrates that DTG Mj can be pushed down by W-scaling at the cost of power, at relatively constant FoM.

As both power and mismatch comparisons are device size dependent, we compare FoM to get a size independent comparison. The FoMs are compared in Figure 3.7. Deviations in FoM exist up to about a factor of two, however the difference between the two logic families is significantly more than the model error. In this comparison, the routing’s parasitic capacitances are not considered. The effect of the parasitic capacitance changes the load ratio and the comparison still can be done from Figure 3.7. Moreover, the effect of parasitic
Figure 3.8: DTG, CML-MPCG FoM vs. frequency ($r_l = 1$ and $C_l = 10 \text{ fF}$)

Figure 3.9: FoM ratio with changing $N$

capacitance reduces as the load ratio increases. Expressed analytically, the FoM-ratio can be found from (3.13) and (3.20):

$$\frac{F_{oM_{CML-FF}}}{2F_{oM_{DTG-FF}}} = \frac{\mu (V_{OD})^4}{2f_o V_{DD}^3 L^2} \cdot \frac{F_{CML}}{F_{DTG}} \cdot \frac{\left[ \frac{4A_{21}^2}{V_{Tn}^2} + A_{K_n}^2 + \frac{3A_{21}^2}{r_{RM}} \right]}{4 + d_{21}^2 A_{V_Tn}^2 + (1 + d_{21}^2) A_{K_n}^2}$$

(3.22)

taking into account that a DTG-MPCG needs $N$ FFs whereas the CML-MPCG needs only
3.3. Comparison of MPCG with DTG-FF and CM-FF

Figure 3.10: Simulated FoM for fixed $C_{in}$ and $C_L$

Table 3.2: Comparison of MPCG for $C_L = 50\ fF$ and $N = 4$ (simulations)

<table>
<thead>
<tr>
<th>Parameters</th>
<th>DTG, $r_l = 1$</th>
<th>DTG, $r_l = 1/8$</th>
<th>CML, $r_l = 1$</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Delay</td>
<td>19</td>
<td>17</td>
<td>22</td>
<td>ps</td>
</tr>
<tr>
<td>$P_d$</td>
<td>6</td>
<td>67.4</td>
<td>42.5</td>
<td>mW</td>
</tr>
<tr>
<td>$M_j$(std.)</td>
<td>54.5</td>
<td>18.8</td>
<td>87</td>
<td>$f s$</td>
</tr>
<tr>
<td>FoM</td>
<td>17.5</td>
<td>23.7</td>
<td>321</td>
<td>$W \cdot f s^2$</td>
</tr>
</tbody>
</table>

N/2 (see Figure 3.1 and 3.3). The ratio in (3.22), say $R_{FoM}$, can also be written as:

$$R_{FoM} = \frac{\pi f_T V_{OD}^5}{f_0 V_{DD}^2 V_S^2} \cdot \frac{F_{CML}}{F_{DTG}} \cdot \frac{4A_{V_{Trn}}^2 + V_S^2 A_K^2 + (3V_S^2 A_R^3)/r_{RM}}{(4 + d_o^2)A_{V_{Trn}}^2 + V_{OD}^2 (1 + d_o^2)A_K^2}$$

(3.23)

where $f_T$ is nMOS unity gain frequency, defined as:

$$f_T = \frac{\mu g_m}{2\pi C_{gs}} = \frac{\mu V_{OD}}{2\pi L^2}$$

(3.24)

In (3.23) the ratio of the FoMs can be separated in three parts: the first term has strong technology dependence and its proportional to $f_T$. With CMOS technology downscaling the $f_T$ increases, and so does the ratio, explaining why DTG MPCGs indeed become relatively better compared to CML in scaled CMOS technologies for a given operating frequency. The second term is a function of design parameters related to circuit topology. The low
capacitance in a DTG-FF as there is no cross-coupled pair, and its fast path from clock
to output helps to boost the ratio through smaller $F_{DTG}$. The third term in (3.23) is a
function of the mismatch parameters and is close to one in most practical cases where
the threshold voltage and K mismatch together is higher than the resistor mismatch, so it
does not affect the comparison result significantly. Figure 3.8 shows this advantage for
wide output frequency range. In this case the simulation was done for a load capacitance
of 10 fF and $r_l = 1$. For the DTG, maximum achievable output frequency is 2.6 GHz i.e.
input frequency of 10.4 GHz. When we change the number of phases, we can either choose
to keep the input frequency or the output frequency constant. From (3.23) FoM ratios for
both scenarios are plotted in Figure 3.9 for $f_o=100$ MHz and $f_i = 4$ GHz. DTG-FF performs
better (ratio > 1).

In Figure 3.10 we compare the simulated FoM for changing FF sizes, with fixed input
(at INCLK+ and INCLK- in Figure 3.1 and 3.5) and output capacitances, also shows an
order of magnitude better FoM for DTG. In this case, extra buffers have been added in the
clock path when larger FF devices are used. Although the CML-FF FoM is more robust
to temperature (5% for -10 to 85°C) and process variations (≈ 15%) than the DTG-FF
(≈ 10% and 55% respectively), a big advantage remains. Therefore for low power and jitter
performance, DTG logic is preferred for wide-band operation, e.g. for flexible software
defined radio applications. This is because its power and FoM are automatically reduced
for lower frequency (1st term in (3.13)) whereas CML always dissipates the current that
required at the highest frequency of operation.

### 3.4 Conclusions

DTG and CML flip-flops have been compared fundamentally with respect to their potential
to realize accurate multi-phase clocks in a power efficient way. The comparison is based on
a FoM which quantifies the product of mismatch-induced timing jitter variance and power
dissipation, normalized for admittance scaling effects. First order analytical expressions
are derived and confirmed by simulations to model mismatch jitter, power dissipation and
Jitter-Power FoM. The analytical expressions are used to compare flip-flops and also to
design them for low FoM. Comparison shows that DTG flip-flops outperform CML in
Jitter-Power FoM in 90 nm CMOS technology. This is mainly because DTG flip-flops
only consume power during switching. Moreover, they have less capacitance (no need for a
cross-coupled pair) which reduces both power and jitter. The advantage scales roughly with
$f_T/f_O$ so technology scaling benefits DTG logic compared to CML (3.23). Although the
3.4. Conclusions

DTG MPCG stops operating after a certain frequency limit (input frequency of 10.4 GHz in this case) beyond which CML is still better, as the technology scales down, this limit of highest frequency will go up, and in future DTG is expected to be better than CML till even higher frequency limit. These comparison and equations can be useful in selecting flip-flops for multiphase generation, for different technologies and frequencies of operation.
Chapter 4

Chirped-LO based Interference Robust Communication

4.1 Introduction

There is a significant amount of literature, such as [33, 46, 76, 77, 78] targeted at the reduction of communication energy of wireless sensor networks (WSNs) and the increase of system battery lifetime. However, interference robustness is not addressed that much even though communication in most WSNs takes place in the largely crowded ISM frequency bands [27]. A global ISM band in the frequency range from 2.4 GHz to 2.5 GHz is widely chosen for WSNs as a good trade-off between antenna size and power consumption. This band of frequency is highly occupied by applications such as WLAN, Zigbee, Bluetooth, cordless telephony, wireless USB, microwave ovens etc. Sensor networks, therefore have to co-exist with one or more of these short range radio standards. A serious effect of the interference can occur if proper care is not taken into account [79]. Hence robustness against interfering signals from various standards is necessary for reliable communications between sensor nodes.

Basic binary modulation techniques are generally used in wireless sensor radio transceivers because of simple and comparatively low power transceiver architectures. Among the binary modulation techniques, FSK and PSK schemes are most interference robust [80]. However, those techniques are prone to in-band interferences [48].

Though interference robustness is a common challenge in various wireless communication systems, it is even a bigger challenge in wireless sensor network applications. Interference robust schemes and mitigation techniques which add a significant amount of power, can be used in other high-performance communication systems but not
in sensor networks because of limited energy resources. Therefore there is a need for simplified robustness schemes which do not increase power consumption considerably but trade-off other performance metrics such as bandwidth efficiency or number of channels. In this chapter we investigate the use of the chirped-clock direct modulation scheme to improve the interference robustness for FSK and PSK transceiver systems. The investigation is limited to determining the BER performance against channel noise and interference power for idealized transceivers. This chapter is built with the improved content of [48], some additional simulation results, and an additional sub-section describing chirp history and theory.

Among the ISM band standards, Wi-Fi (Wireless LAN) transmits signals with a bandwidth of at most 22 MHz. All other signals are comparatively narrow band. Therefore, a narrow-band rejection scheme will still be effective against interference from most of the standards.

The structure of this chapter is as follows: Section 4.2 provides a brief history of chirped communication and chirped clock basic theory. After that in Section 4.3, chirped-FSK and chirped-PSK systems are proposed and their advantages are shown with a simple BER model and supported by simulation results in Section 4.4. Then conclusions are drawn in Section 4.5.

### 4.2 Spread Spectrum using Chirped Clock

Spread spectrum techniques are useful to mitigate narrow band interference effects [41, 42]. The most popular spread spectrum techniques, direct sequence spread spectrum (DSSSS) and frequency hopping spread spectrum (FHSS) can achieve high performance but at the cost of high power consumption and/or higher complexity as argued in Chapter 1, Section 1.3.4 [43, 44]. Another technique, called chirped spread spectrum, is used for RADAR. In this case, spreading and de-spreading of the signal in the transmitter and receiver is done using devices such as surface acoustic wave (SAW) filters. There are several potential advantages of using a chirp signal as a means of wireless transmission. A chirp signal has the ability of pulse compression [81], which helps to transmit over greater distances without increasing transmitter power. For that reason it finds application in RADAR and SONAR. It has a potential to be used for precise ranging needed for WSN localization [82]. Other applications of chirp signals are in Doppler shift measurement [83].
4.2. Spread Spectrum using Chirped Clock

4.2.1 History of chirped communication

The use of the chirped signal for pulse compression was invented during World War II and later published by Cook [84] and Klader [85] in 1960. Chirp modulation for communication was first proposed by Winkler in 1962 [86] using Binary Orthogonal Keying (BOK). There are several publications on the theory and advantages of chirp communications, such as [87], where chirp modulation was proposed to combat multi-path propagation. The use of Surface Acoustic Wave (SAW) filters to generate chirped signals is first proposed by Bush in [88]. However, in a highly multi-path fading environment, there is a requirement of a pulse duration of at least more than the excess delay, i.e. the difference between the maximum and the minimum propagation delays among all significant signal paths. Due to the lack of SAW filters which can generate pulses with longer duration [89], the usage and research activity of the chirped spread spectrum technique was taken over by other spread spectrum techniques. However for indoor communications with less excess delay, chirp communication becomes practical. In 1994, a BOK system for indoor communication is proposed in [90] using a SAW filter.

4.2.2 Chirped Communication: BOK vs. Direct Modulation

In chirp BOK modulation, the binary data is represented by a chirped clock signal with opposite sign of frequency change rate with respect to time (also called chirp-rate). For instance, a ‘1’ can be represented by a positive chirp-rate and a ‘0’ can be represented by a negative chirp-rate. The BER of a BOK system is approximately equal to the BER of an ideal non-coherent BFSK system with orthogonal frequencies. However, BOK systems have problems with cross correlation of the symbols [89] which degrades the BER performance. Also BOK systems can not achieve a high data-rate because the chirp time of BOK is the same as the bit period and chirp-time can not be too short because of time-bandwidth product limitation. Direct modulation of a chirp system can solve these problems of BOK.

Direct modulation was first proposed in [91] for differential phase shift keying (DPSK) modulation. In direct modulation, chirps are only used for spreading and de-spreading instead of representing symbols. The modulation and demodulation processes are separated from the spreading and de-spreading processes. Therefore many modulation schemes can be used along with the chirp. Direct chirp modulation can be implemented in two ways; by filters or by oscillators. A simplified block diagram of a direct chirp modulation system using filters is shown in Figure 4.1. In this system, the modulated signal is passed
through an up or down chirp filter to spread the signal. In the receiver the opposite filter is used before demodulation. The filters are generally implemented by SAW devices. A detailed description of chirped communication by BOK and by direct modulation using SAW devices is given in [89].

In the other variant of the direct modulation scheme, chirping is performed by oscillators [92] (See Figure 4.2). This mechanism has several advantages over the filter implementation. An external SAW device is not very suitable for wireless sensor node transceivers which intend to be as small as possible in size. Moreover a SAW device can add a loss as large as 20 to 30 dB [93]. Instead of filters, active chirp generation is performed by an oscillator, for example by controlling the input of a Voltage Controlled Oscillator (VCO). As shown in Figure 4.2, the RX and TX Local Oscillators (LO) can be chirped.
4.2. Spread Spectrum using Chirped Clock

in a similar fashion to obtain chirped communication. This method is much more flexible than using a dedicated filter. The chirp-rate, center frequency and even whether to use the chirped or non-chirped clock, can be programmed (i.e. the same system can be transformed to a narrow-band system by software). Furthermore, a high chirp-rate and high datarate can be obtained in this method [89]. This method is used in the remainder of this thesis and is referred to as *chirped-LO* communication.

4.2.3 Chirped Clock Theory

![Figure 4.3: An up-chirp example waveform; amplitude vs. time (top), frequency vs. time (bottom)](image)

A clock is called "chirped" when the frequency of the signal is changing with time. For a linear chirp, the rate of frequency change is constant. Example linear up-chirp time-amplitude and time-frequency plots are shown in Figure 4.3. As indicated in the figure, $B_{CH}$ is the chirp-bandwidth and $T_{CH}$ is the time duration of one single chirp (say chirp-time). The angular frequency of this chirp signal as a function of time $t$, can be represented as:

$$\omega_{up}(t) = 2\pi[f_{S} + \beta \{(t \mod T_{CH}) - \theta\}]$$  \hspace{1cm} (4.1)

where $\beta = B_{CH}/T_{CH}$, is the rate of frequency change with time or the chirp-rate, $f_{S}$ is the lower/starting frequency, $T_{CH}$ is the chirp-time, $\theta$ is the initial phase of the chirp repeat
cycle (See Figure 4.3), and mod is the modulo operator. Without loss of generality, the initial phase and the time spent in previous cycles can be ignored. Therefore (4.1) can be simplified for a single chirp to:

\[
\omega_{up}(t) = 2\pi(f_S + \beta t)
\] (4.2)

For the up-chirp, the instantaneous phase, using (4.2) can be derived as:

\[
\phi_{up}(t) = \int \omega_{up}(x)dx = 2\pi f_S t + \pi \beta t^2 + \phi_1
\] (4.3)

where \(\phi_1\) is the initial phase of the signal. Therefore the up-chirp signal, with amplitude \(A\), can be represented as:

\[
s_{up}(t) = A \cos(2\pi f_S t + \pi \beta t^2 + \phi_1)
\] (4.4)

Similarly a down-chirp can be represented as:

\[
s_{down}(t) = A \cos(2\pi f_E t - \pi \beta t^2 + \phi_1)
\] (4.5)

where \(f_E\) is the maximum/ending (up-chirp convention) frequency of the linear chirp. For an up-down chirp, of which two are shown in Figure 4.4a, the starting frequency is different for the up and down parts of the chirp. Omitting the mod operator for better readability, an up-down chirp signal can be represented as:

\[
s_{ud}(t) = \begin{cases} 
A \cos(2\pi f_S t + \pi \beta t^2 + \phi_1) & \text{when } \left\lfloor \frac{t}{T_{CH}} \right\rfloor \text{ is even} \\
A \cos(2\pi f_E t - \pi \beta t^2 + \phi_1) & \text{when } \left\lfloor \frac{t}{T_{CH}} \right\rfloor \text{ is odd}
\end{cases}
\] (4.6)

### 4.2.4 Chirped-clock Spectrum

The spectrum of a chirped clock is analyzed in [81, 89]. To use similar expressions as used in [89], without loss of generality, an up-chirp signal is assumed to be present between \(t = -T_{CH}/2\) to \(t = T_{CH}/2\). The spectrum of this up-chirp signal can be written as:

\[
S(f) = A(f) \exp(-j\phi(f))
\] (4.7)
4.2. Spread Spectrum using Chirped Clock

Figure 4.4: Up-down chirp (a) frequency vs. time plot and (b) spectrum; \( B_{CH} = 100 \text{ MHz}, \ T_{CH} = 2 \mu s, \) Time Bandwidth Product = 200, Power within \( B_{CH} = 99.5\% \).

where the amplitude and phase spectrum are expressed as:

\[
A(f) = \frac{1}{B_{CH}} \sqrt{2T_{CH}B_{CH} \left \{ \left [ C(x_1) + C(x_2) \right ]^2 + \left [ S(x_1) + S(x_2) \right ]^2 \right \} } \tag{4.8}
\]

\[
\phi(f) = \frac{T_{CH} B_{CH}}{2} \left ( \frac{f_c - f}{B_{CH}} \right )^2 - \arctan \left [ \frac{S(x_1) + S(x_2)}{C(x_1) + C(x_2)} \right ] \tag{4.9}
\]

where \( f_c = \left ( f_s + B_{CH} / 2 \right ) \) is the center frequency of the chirp, the functions \( S(.) \) and \( C(.) \) are representing the Fresnel sine and cosine integral, \( x_1 \) and \( x_2 \) are functions of \( f \), and given by

\[
x_1(f) = \sqrt{2T_{CH}B_{CH} \left \{ 0.5 + \frac{f_c - f}{B_{CH}} \right \}} \tag{4.10}
\]

\[
x_2(f) = \sqrt{2T_{CH}B_{CH} \left \{ 0.5 - \frac{f_c - f}{B_{CH}} \right \}} \tag{4.11}
\]

The time-bandwidth product (TBP) determines the spectral response of a chirp waveform. For a large time-bandwidth product, the amplitude spectrum of the chirp signal can be approximated by a rectangularly shaped spectrum [89]. For example for both up-chirp and up-down chirp with a TBP of 100 or higher, more than 98\% of the signal power remains within the chirp bandwidth \( B_{CH} \). For a TBP of 200, the spectral responses of an up-down-chirp and an up-chirp are shown in Figures 4.4(b) and 4.5(b) respectively. As can be seen from the figures, up-down chirp spectrum out-of-band power is much lower than the up-only/down-only chirp spectrum plot. The time-bandwidth product is an important performance parameter of chirped spread spectrum communication and is also called processing gain [43] or dispersive factor.
4.3 Chirped-FSK and Chirped-PSK Modulation

The chirped-LO for the receiver and the transmitter are assumed to be synchronized in this thesis. The chirped-LO is combined with some low power modulation schemes suitable for WSNs application. Binary modulation schemes, usually consume less power because of their simplicity and are often used for WSNs radios (Table 1.5). As BFSK and BPSK are more robust than OOK modulation [29, 94], they are chosen in the proposed chirp direct modulation scheme of this section. A chirped clock is used as a carrier frequency and both FSK and PSK modulation schemes are analyzed. In case of FSK modulation and concentrating on the up-chirp part, the ‘1’ and ‘0’ bits of the message can be represented by two up-chirps with the same frequency-time slope, with frequency $f_1$ and $(f_1 + \Delta f)$ respectively. The corresponding signals can be written as:

$$s_{FSK}(t) = \begin{cases} 
A \cos(2\pi f_1 t + \pi \beta t^2 + \phi) & \text{when } m(t) = 1 \\
A \cos(2\pi (f_1 + \Delta f)t + \pi \beta t^2 + \phi) & \text{when } m(t) = 0 
\end{cases} \quad (4.12)$$

The modulated signal is switched between those two chirps depending on the message, $m(t)$. Similarly, the modulation of a down-chirp can be defined and based on that the combination can be obtained. The FSK modulated signal for up-down chirp is shown in Figure 4.6 [48]. The green and blue lines in the figure indicate the frequency for the two
4.3. Chirped-FSK and Chirped-PSK Modulation

Possible signals of binary FSK (BFSK). The red line indicates the frequency change of the chirped-FSK modulated signal; switching between the two frequencies. Although the up-down chirps have better spectral purity and are shown in the figure, the up (or down) chirp TRX implementation is more power efficient which will be clear later in the thesis. Therefore, as the target of the thesis is a low power system, in this thesis only an up-chirp is used for the analysis and later for simulations. The up-chirp FSK modulation curve is not added assuming it can be extracted from up-down chirped FSK curve of Figure 4.6. A block diagram of an ideal modulator is shown in Figure 4.7. Here the chirped clock is indicated by the input of the voltage controlled oscillator, as a practical method for chirped clock generation.

4.3.1 Chirped-coherent FSK Demodulation

Among the two basic FSK receiver types, i.e. coherent (CFSK) and non-coherent (NCFSK), the coherent receiver needs phase synchronization. It is assumed that the exact chirp clocks, as expressed in (4.12) are available in the receiver after proper frequency and phase synchronization. The ideal binary CFSK receiver, based on correlation and integration over symbol time \( T_b \) is shown in Figure 4.8. This architecture provides optimum CFSK demodulation. The probability of error (or bit error rate) of detection resulting from this
CFSK receiver in the presence of white Gaussian noise can be expressed as [95]:

\[
\text{BER}_{\text{CFSK}} = Q\left(\sqrt{\frac{E_b}{N_0}}\right)
\]

(4.13)

where \(E_b\) is the energy per bit and \(N_0\) is the power spectral density of white Gaussian noise and \(Q(x)\) is defined as:

\[
Q(x) = \frac{1}{2\pi} \int_{-\infty}^{\infty} \exp\left(-\frac{u^2}{2}\right) du
\]

(4.14)

The ratio \(E_b/N_0\) is the same as the signal to noise ratio (SNR) in power domain assuming the signal data rate and noise bandwidths have same value. An idealized system is assumed here to simplify the analysis.

To analyze the interference effect on the chirped-CFSK system, we assume that partial-band Gaussian random interference with zero mean and flat power spectral density (noise-like) is added to the channel. This interference is assumed to be present in a fraction of the total chirp bandwidth and absent (zero power) everywhere else. The noise-like interference over the carriers of an FSK signal increases the noise level and hence increases the error probability. Assuming an interference power spectral density of \(I_0\), we can modify the probability of error for CFSK in the presence of interference without chirping the carrier as:

\[
\text{BER}_{\text{CFSK}_I} = Q\left(\sqrt{\frac{E_b}{N_0 + I_0}}\right)
\]

(4.15)
4.3. Chirped-FSK and Chirped-PSK Modulation

Figure 4.8: Chirped CFSK receiver realized by replacing the LO of a standard coherent receiver by chirped-LO.

Let’s say the interference bandwidth is $B_i$, and the ratio of interference bandwidth to chirp bandwidth ($B_i/B_{CH}$), is $r_W$. For chirped-CFSK, assuming the frequency difference, $\Delta f$ is much smaller than $B_{CH}$, the receiver will only be affected by interference with approximate probability of $r_W$ and will not be affected for the rest of the probability of $(1 - r_W)$. So the probability of bit error in the presence of interference can be approximated as:

$$ BER_{CH\_CFSK\_I} = r_W \cdot Q\left(\sqrt{\frac{E_b}{N_0 + I_0}}\right) + (1 - r_W) \cdot Q\left(\sqrt{\frac{E_b}{N_0}}\right) $$

(4.16)

The ratio $\frac{E_b}{I_0}$ can be related to the Signal to Interference Ratio (SIR) as,

$$ \frac{E_b}{I_0} = \frac{P_S T_b}{I_0} = \frac{P_S R}{I_0 / B_i} = \frac{SIR B_i}{R} $$

(4.17)

where signal and interference power are defined as $P_S$ and $P_i$ respectively and their ratio (SIR) is the signal to interference ratio, $T_b$ is the bit period and $R$ is the datarate. Using this, (4.16) can also be written as:

$$ BER_{CH\_CFSK\_I} = r_W \cdot Q\left(\sqrt{\frac{1}{SNR^{-1} + SIR^{-1} R B_i}}\right) + (1 - r_W) \cdot Q\left(\sqrt{SNR}\right) $$

(4.18)

From (4.18) it can be seen that the chirping can improve BER using a lower value of $r_W$, i.e. $B_{CH} >> B_i$. At a very low value of $r_W$, the interference effect can be almost neglected.
4.3.2 Chirped non-coherent FSK Modulation

Coherent FSK demodulation has the disadvantage that it needs time consuming phase synchronization. Spending more time on synchronization means more energy consumption. One solution for this problem is to use non-coherent FSK (NCFSK) detection. An NCFSK receiver using two band-pass filters [96] is not a practical solution because of the very high-Q filter requirement. Another NCFSK demodulator uses a quadrature clock as shown in Figure 4.9 [95]. The probability of error of ideal NCFSK detection is given by [96]:

\[
BER_{CH, NCFSK} = \frac{1}{2} \exp \left( -\frac{1}{2} \frac{E_b}{N_0} \right)
\] (4.19)
In the presence of interference and using a chirped clock for all the clock generators in Figure 4.9, the Bit Error Ratio (BER) can be calculated similar to CFSK (4.18):

\[
\text{BER}_{\text{CH,NCFSK,I}} = \frac{r_w}{2} \exp \left( \frac{-1}{2 \left(\text{SNR}^{-1} + \text{SIR}^{-1} \frac{R}{B_i} \right)} \right) + \frac{1 - r_w}{2} \exp \left( \frac{-1}{2 \text{SNR}} \right) \tag{4.20}
\]

4.3.3 Chirped BPSK modulation

Binary phase shift keying (BPSK) is another popular modulation scheme with a better BER performance compared to the BFSK [96]. For chirped-BPSK, two up-chirped clock signals with opposite phases are used as the modulating signal. The phase difference between those two signals is \( \pi \) radians, the same as in conventional BPSK modulation. The chirped BPSK modulated signal can be represented as:

\[
s_{\text{PSK}}(t) = \begin{cases} 
A \cos \left[ 2\pi f_s t + \pi \beta t^2 + \pi \right] & \text{when } m(t) = 1 \\
A \cos \left[ 2\pi f_s t + \pi \beta t^2 \right] & \text{when } m(t) = 0 
\end{cases} \tag{4.21}
\]

where \( f_s \) is the starting frequency of both chirped-LO signals. Note that in 4.21 \( t \) should actually be ‘\( t \mod T_{CH} \)’, but for the reasons of better readability this ‘\( \mod T_{CH} \)’ part is dropped here. A chirped BPSK transceiver architecture is shown in Figure 4.10. In the TX, a chirped BPSK modulated signal is generated by switching between two chirped-LO signals with a phase difference of \( \pi \) radians. In the RX, the incoming signal is multiplied with a synchronized LO signal and subsequently integrated over a bit period. Only one correlator is needed in this RX whereas for the FSK RX either two or four correlators are required. However, it also needs both phase and frequency synchronization for proper operation. Assuming appropriate phase and frequency synchronization is performed, the bit error probability in the presence of white Gaussian noise can be written as [96]:

\[
\text{BER}_{\text{BPSK}} = Q \left( \sqrt{\frac{2E_b}{N_0}} \right) \tag{4.22}
\]

The effect of interference on chirped-BPSK system can be estimated as derived for the chirped-coherent FSK demodulation (Section 4.3.1). The error probability when a chirped clock is used in BPSK, can be written as (using the same interferer assumptions
Chapter 4. Chirped-LO based Interference Robust Communication

Figure 4.10: Chirped binary PSK transceiver architecture based on correlators

as in (4.3.1)):

\[
BER_{CH_{BPSK}} = r_W \cdot Q \left( \frac{2}{SNR^{-1} + SIR^{-1} \frac{R}{B_I}} \right) + (1 - r_W) \cdot Q \left( \sqrt{2 \cdot SNR} \right)
\] (4.23)

From the BER equations of the FSK and PSK systems, it is clear that with the increase of chirped-LO bandwidth, the interference robustness increases and the improvement is more when the system is dominated by interference compared to noise.

4.3.4 Discussion

From (4.18), (4.20) and (4.23), it can be seen that the chirped-LO scheme can reduce the interference effect on BER. For all three cases, the BER improvement due to LO chirping is proportional to the bandwidth ratio, \( r_W \) in a interference dominated situation. Because of the similarity in robustness, one of these three architectures will be selected for implementation in the next chapter, based on energy efficiency only. In the next section, simulation results are shown to confirm the prediction done by these simplified equations.

Please note that timing synchronization of the bit/symbol period is needed for all communication systems. In chirped-LO transceivers, timing synchronization is needed for both the chirp and the symbol clock. As the chirp and symbol clock can be aligned in the proposed system, synchronization of the chirp clock can be used to synchronize both the chirped LO and the bit/symbol clock. Therefore, the timing synchronization requirements in this system are shifted to the chirp clock instead of the bit clock and are not expected
to add a big overhead compared to narrow-band systems. Our research so far shows that efficient chirp synchronization schemes are feasible by looking at the frequency difference between transmitter and receiver [97]. In Appendix- B, a chirped-LO synchronization procedure using an FFT is proposed.

4.4 Simulation results

![Spectrum of the time discrete partial band Interference signal.](image)

To validate the theoretical approximations, the BER performances of the modeled FSK and PSK systems are simulated in MATLAB. To generalize the interference scenario, a partial band of interference is used in the simulation. In this Section first the generation of the interference is illustrated and then the simulation results are described.

4.4.1 Generating partial band noise like interference

For time discrete simulations of the interference robustness of the system, an interference-model is created. White noise like Gaussian interference is generated by a series of narrow-band frequency tones $f_{i_k}$ starting from frequency $f_{i_0}$, where their phase, $\phi_k$ is a uniformly distributed random variable ($0 \leq \phi_k < 2\pi$):

$$s_{PBI}(t) = \sum_{k=1}^{M} A_k \cos \left[ 2\pi \left( f_{i_0} + \frac{B_i}{M} \right) t + \phi_k \right]$$

(4.24)
where $B_i$ is the interference bandwidth and $A_k$ is the amplitude of the k-th interference frequency component. To obtain a flat spectrum, $A_k$ is equal for all $k$, let's assume being $A_i$. Two consecutive sinusoidal tones should have an integer number of cycles in the total number of points. The number of frequency tones required to fill a partial band with interference depends on the sampling frequency and total number of time samples used. If the sampling frequency is $f_{SP}$ and the total number of points in time is $N_s$, then the frequency resolution is $f_R = f_{SP}/N_s$. So, the number of frequency tones to be added for an interfering bandwidth of $B_i$ is:

$$M = \frac{B_i}{f_R} = \frac{B_i}{f_{SP}} \frac{N_s}{f_{SP}} \quad (4.25)$$

For an interference band of 10 MHz in the frequency range between 2.45 GHz and 2.46 GHz ($B_i = 10$ MHz), with sampling frequency, $f_{SP}=10.24$ GHz, and a total number of points $N_s = 2^{22}$, from (4.25) the number of frequency tones to be added becomes $M=4096$. Note that $M$ needs to be a natural number, so the $f_R$ and $f_{SP}$ should be chosen correctly. The corresponding interference is shown in Figure 4.11. The power of the interfering signal plays an important role in the system performance. The average power of $M$ sinusoidal signals with amplitude $A_i$ is: $P_i = \frac{A_i^2}{2}M$. To achieve an interfering power of $P_i$, we need the
4.4. Simulation results

interfering signal amplitude to be:

\[ A_i = \sqrt{\frac{2P_i}{M}} \]  

(4.26)

4.4.2 Chirped-FSK and chirped-PSK results

![Figure 4.13: Simulated and modeled BER comparison: for CFSK and chirped-CFSK in the presence of PBI.](image)

The chirped clocks are assumed to be synchronized between the RX and the TX. In case of FSK systems (CFSK and NCFSK), the frequency difference for a transmitted one or zero is assumed to be 5 MHz. The two FSK carriers for ‘0’ and ‘1’ are at 2.452 GHz and 2.457 GHz. For both FSK and PSK systems, the data rate chosen is 5 Mbps. An interference band of 10 MHz from 2.45 GHz to 2.46 Hz is used. Two interference power levels of -4 dBm (Intf-1) and 10 dBm (Intf-2) are simulated, while the signal power is 0 dBm. For all simulations, the chirp bandwidth is assumed to be \( B_{CH} = 100 \text{MHz} \), from \( F_S = 2.4 \text{ GHz} \) to \( F_E = 2.5 \text{ GHz} \).

At first the chirped and non-chirped systems are simulated only in the presence of channel white noise. As expected, the BER performances of the chirped-LO systems are alike to the corresponding non-chirped systems as shown in Figure 4.12. Therefore it can
be concluded that an idealistic chirped-LO system performs the same as the corresponding non-chirped system in the presence of white noise.

Then the interference is added in the channel and chirped and non-chirped system performance are compared. Figure 4.13 shows the simulated and modeled BER for the CFSK and chirped-CFSK (equation (4.16)) communication for both intf-1 and intf-2. As it can be observed, the conventional CFSK performances are more affected by interference compared to the chirped-CFSK performances. The simulated results match well with the simplified BER model. Similarly, Figure 4.14 shows the simulated and modeled BER for the NCFSK and chirped-NCFSK communication. In this case however, the model predicts lower BER for low interference and for high interference the model predicts higher BER than the simulation. However, the modeled BER matches reasonably well with the simulated result.

The PSK system shown in Figure 4.10 is simulated in MATLAB as well. One single frequency of 2.45 GHz is used for the PSK modulated signal. Interferences with similar characteristics (as used for FSK) are added to the channel. The simulated and modeled BER performances are plotted in Figure 4.15. In the presence of interference, the BER
4.5 Conclusion

is more severely degraded for BPSK as compared to chirped-BPSK. The BER model gives a reasonably close approximation as can be seen from Figure 4.15. The simulation results illustrate that by using a chirped carrier, the interference robustness of the FSK and PSK systems can be improved. Please note that the advantage of using chirping changes significantly with $r_W (=0.1$ here). Simulation results with other values of $r_W$ can be interesting; however similar results are expected and greater focus is directed on the design and implementation of the ultra low energy receiver circuits presented in the next Chapter.

4.5 Conclusion

To achieve higher interference robustness, a modulation scheme is proposed where the RF transmission frequency is chirped by a chirped-LO both in receiver and transmitter. This spectral spreading method, also called direct chirp modulation, is chosen because of potentially simpler hardware implementation and possible ultra low power operation. With this chirped-LO scheme, modulation and demodulation methods of FSK and PSK
are described. Compared to the conventional CFSK, NCFSK and PSK systems, ideal chirped-CFSK, chirped-NCFSK and chirped-PSK systems respectively show similar performance against channel noise. The effects of non-idealities such as phase noise, frequency nonlinearity and drifts of LO are not considered here. The BER of chirped systems are also compared with the non-chirped system in the presence of partial band interference. In this case, chirped communication shows better BER performance than non-chirped communication for CFSK, NCFSK and PSK systems. A simplified BER model is developed, which can match the simulated BER performance with a reasonable accuracy. These results exhibit that a chirped-LO spread spectrum modulation can provide robustness against interference close to the carrier for both FSK and PSK systems.
Chapter 5

Ultra Low Power/Energy Interference Robust Receiver IC Implementation and Measurement Results

5.1 Introduction

As discussed in Chapter 1, most applications of wireless sensor networks (WSNs) require an ultra low energy (ULE) radio to extend battery life [27], so that no or minimum maintenance is required after initial installation. As mentioned in Chapter 2, sensor node battery life time can be increased by duty-cycling the radio transceiver [76]. When duty-cycling is used, energy/bit reduction should be the primary target in a wireless sensor network radio to increase battery lifetime. Therefore this chapter deals with the design of an ultra low energy receiver that targets a very low energy/bit. This chapter is entirely same as [49], except some minor text changes and improvements.

Several low power receivers are reported in literature [29, 31, 32, 33, 34, 35, 36, 37, 98]. However, most of these receivers operate at low data rate and thereby do not exploit the duty-cycling effectively to minimize the energy-per-bit performance. In Chapter 4, it was presented that the overall energy consumption for the transmission of a fixed number of bits can be reduced by choosing a proper data-rate and receiver noise figure [46]. Although the optimum choice depends on link budget, technology, MAC protocol etc., a relatively high data rate (compared to the one commonly used for sensor networks) is preferable to quickly transfer the required data between the transmitter and receiver, and then both can go to sleep mode.

In Chapter 4, it was stressed that interference robustness is necessary in a WSN
because of its operation in a unlicensed frequency band such as the 2.45 GHz ISM band. Spread spectrum techniques can provide good robustness against interference [44]. For example the Ultra Wide Band (UWB) transceivers reported in [99, 100] are very robust to in-band interference. However, these UWB receiver consume too much energy to be used for ULE communication. The ultra low power receiver in [29] is more interference robust than conventional ON-OFF Keying (OOK) receivers due to the use of a 2-tone RF carrier. However, interferer tones at specific frequencies still create a problem similar to a conventional Binary Frequency Shift Keying (BFSK) receiver. In [29], the minimum in-band SIR achieved is -7 dB with a transmitted reference scheme, however at the cost of comparatively higher energy-per-bit. To the best of the authors’ knowledge, no ULE radio features in-band interference robustness independent of the frequency of the interferer at the time of publication [49].

Simulations in Chapter 4 indicate that chirped clock transceivers can enhance interference robustness against in-band interference [48]. Among the spectrum spreading techniques, this method is flexible, simple and has a potential for low power operation. In this chapter we demonstrate that chirped clock communication can be achieved in an ULE receiver suitable for wireless sensor networks. Energy reduction is achieved by using low power circuit techniques and choosing optimum data-rate and noise-figure [46]. Based on the calculations in Chapter 2, a data rate of 8 Mbps and noise figure of 18 dB is chosen with the help of technology and some estimated circuit parameters. A new 3-phase receiver architecture helps to minimize oscillator and mixer power consumption compared to conventional BFSK quadrature receivers. Proper choice of architecture, IF amplifiers, and a new low-power BFSK demodulator also help to reduce power consumption further.

5.2 Chirped-clock Receiver and Interference Effects

Chirped clock signals have been shown to have a better in-band interference robustness for FSK and PSK in Chapter 4 [48]. In this chapter, an up-chirp binary FSK modulation in an ultra low power direct conversion receiver is proposed.

An up-chirp signal is shown in Figure 5.1 where the number of bit periods in one chirp period, \( n_b = 4 \). The bit periods are aligned with the chirp time, such that symbol synchronization can be derived from the chirp synchronization. For each bit, the chirp bandwidth is \( b_{CH} = (f_E - f_S)/n_b = B_{CH}/n_b \), where \( B_{CH} \) is the total chirp bandwidth, \( f_S \) is the start frequency and \( f_E \) is the end frequency of the chirp. The transmitter and receiver chirp have to have the same characteristics: \( f_S \), \( B_{CH} \), and the chirp time period (say \( T_{CH} \)).
5.2. Chirped-clock Receiver and Interference Effects

The product of $B_{CH}$ and $T_{CH}$ is called the time-bandwidth product of the chirp. To keep the chirp signal power inside the specified bandwidth, the time-bandwidth product should be $\geq 100$ [89].

The effect of using a chirped-LO signal in the presence of a single tone interference (STI) is illustrated in Figure 5.2. Signal amplitudes are not shown in the figure for compactness. Both TX and RX LO frequencies are chirped having the same characteristics. The modulated received signal can have one of the two possible starting frequencies depending on the data. For simplicity it is assumed here one data (either ‘0’ or ‘1’) is continuously transmitted. Assuming a zero initial phase, a unit-power up-chirp clock can be represented as:

$$c(t) = \sqrt{2}\cos(2\pi f_S t + \pi \beta t^2)$$  \hspace{1cm} (5.1)

where $f_S$ is the LO chirp starting frequency, $\beta$ is the frequency-time slope = $B_{CH}/T_{CH}$. This is the in-phase LO signal of the quadrature receiver. As the LO power have similar effect on the signal and interference, it is assumed to be unity without loss of generality.

Let’s assume the received signal $r(t)$ is comprised of a desired signal $s(t)$, defined in (5.2)

$$s(t) = \sqrt{2P_s}\cos(2\pi f_{R} t + \pi \beta t^2)$$  \hspace{1cm} (5.2)

and an interfering signal $i(t)$, represented in (5.3).

$$i(t) = \sqrt{\frac{2P_s}{\alpha}}\cos(2\pi f_i t + \phi_i)$$  \hspace{1cm} (5.3)

where $f_R$ is the starting frequency of the received RF chirp signal, $P_s$ is the input signal
Chapter 5. Ultra Low Power/Energy Interference Robust Receiver IC Implementation and Measurement Results

Figure 5.2: Single tone interference response of chirped LO direct conversion BFSK receiver. Signal amplitudes are not shown for compactness. One of the BFSK tones is shown assuming one bit (either ‘0’ or ‘1’) is continuously transmitted.

Power and $\alpha$ is the signal to interference power ratio. The instantaneous phase of the input signal, the interference and the LO signals can be assumed to be zero as a phase offset does not affect the performance in a non-coherent receiver. After down conversion by the mixers, the desired signal will generate the required tone with frequency ($f_{IF} = f_R - f_S$) (only the positive part of the frequency is shown for the sake of simplicity). However, the interferer signal goes through spectral spreading as shown in Figure 5.2. Therefore the low pass filter can reduce the interference power and thus reduce the effect of the interference on the BER. It can also be visualized as if the passband frequency of the effective RF bandpass filter due to the IF low pass filter is shifting along with the chirped-LO over time. Therefore, the interference can be rejected by IF filtering if the chirp bandwidth is high enough.

To see the advantage in the BER for the chirped-clock communication, the BER vs. SNR relation of an ideal non-coherent BFSK receiver [96] is used:

$$BER = \frac{1}{2} \exp \left( -\frac{1}{2} \frac{E_b}{N_0} \right) = \frac{1}{2} \exp \left( -\frac{1}{2} \frac{P_s}{P_n} \right)$$

(5.4)

where $E_b$ is the signal energy per bit, $N_0$ is the noise power spectral density and $P_n$ is the white Gaussian noise power. As the interference power is spectrally spread after down conversion, similar to the white noise we use the BER relation to the SNR given in (5.4) to estimate the relation between the BER and the Signal to Interference Ratio (SIR). Here
5.2. Chirped-clock Receiver and Interference Effects

an interference dominated situation where noise can be ignored is assumed. The BER for the chirped clock communication in the presence of a Single Tone Interference (STI) can be expressed as:

$$BER_{ch} = \frac{1}{2} n_b \sum_{n=0}^{n_b-1} \exp \left( -\frac{1}{2} \frac{P_s}{P_i(n)} \right)$$  \hspace{1cm} (5.5)$$

where $P_i(n)$ is the interference power left after the low pass filtering in the receiver for each bit position $n = 0$ to $n_b - 1$. Assuming an ideal brick-wall low pass filter with cut-off frequency, $f_{lpf}$, the interference power will be divided by a factor $b_{CH}/(2 \cdot f_{lpf})$ times. The pass band is approximated to $2 \cdot f_{lpf}$ because the filter passes interference power for both the positive and negative frequencies except when the interference is at the edge of the chirp bandwidth. Therefore for $n_b = 1$, (5.5) can be modified as:

$$BER_{ch} \approx \frac{1}{2} \exp \left( -\frac{1}{2} \frac{B_{CH}}{2 \cdot f_{lpf}} \right)$$  \hspace{1cm} (5.6)$$

On the other hand if a large number of bits are used in a chirp, ($b_{CH}$ is very small and the advantage of spectral spreading in Figure 5.2 is not valid anymore) the BER can be assumed to be affected only in a fraction of the chirp time when the chirped clock is passing through the interference provided $B_{CH} > f_{lpf}$. The transmitted bits will be affected when the chirped-LO is within $\pm f_{lpf}$ of the interference frequency. The fraction of time when the receiver is affected by the interference, approximately equals to $2 \cdot f_{lpf}/B_{CH}$. When the interference is present, however, all interference power is down-converted as $b_{CH}$ is small in this case. Therefore, the BER can be approximated as:

$$BER_{ch} \approx \frac{f_{lpf}}{B_{CH}} \exp \left( -\frac{1}{2} \alpha \right)$$  \hspace{1cm} (5.7)$$

From (5.6) and (5.7), we see that the BER advantage of using a chirp exists for any $n_b$ for a large chirp bandwidth such that $B_{CH} > f_{lpf}$. Due to a steeper reduction for $n_b = 1$, it can achieve highest interference robustness for a given chirp bandwidth, $B_{CH}$ for higher values of SIR. However, maximum achievable data rate can be limited with $n_b = 1$ due to the chirp time-bandwidth product limitation. On the other hand, for a low value of SIR, high $n_b$ value is good as the BER does not increase beyond $\frac{f_{lpf}}{B_{CH}}$ even at a high SIR value. A fractional number of bits in one chirp is also possible but does not help for BER and therefore not considered in this work. The choice of the $B_{CH}$ and $n_b$ values will be done in Section 5.5 by system simulations with the model of the proposed receiver considering LO accuracy,
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filter bandwidth and demodulator performance.

If the co-channel interference is also chirped, the advantage is still present for most interference scenarios. The advantage then depends on the comparative chirp characteristics of the interferer and the LO. Interference tolerance decreases when all characteristics of the LO chirp and the interference chirp are similar. If there is any mismatch of either chirp-slope, starting chirp phase, chirp-time or bandwidth then the robustness increases. If the interference is opposite to the LO chirp (down chirp in this case), then the robustness is better than for single tone interference because the interference then spreads to double the chirp-bandwidth after the down conversion mixer and the low pass filter rejects more interference power. Only when the interference chirp is time-synchronized with the LO and has similar chirp-time and chirp bandwidth, the interference will have the same effect as in narrow-band fixed LO communication. Detailed analysis and simulation of the chirped-LO co-channel interference scenarios can be useful but left for future work partly because a TDMA-only system with one channel is proposed here as described in Section 5.3.1.

As described in Chapter 4, in this Chapter also the chirp clocks are assumed to be synchronized between the transmitter and the receiver and the chirp and symbol clocks are aligned so that chirp synchronization helps symbol synchronization.

5.3 3-Phase Receiver Architecture

The proposed receiver architecture is shown in Figure 5.3. A direct conversion (zero IF) receiver is used as it requires the lowest possible bandwidth in the IF amplifiers resulting in low IF power consumption. Thanks to the BFSK signaling used there is no desired baseband signal at DC and thus high pass filtering can be used in the IF path to eliminate amplifier offsets and reduce the effect of flicker noise.

It will be shown in subsection 5.3.4 that three phases of LO are enough to obtain quadrature (I and Q) baseband output. Therefore, to save power we use a 3-stage ring oscillator, which drives a 3-phase mixer. A low-power flipflop based BFSK demodulator is used which needs in-phase (I) and quadrature phase (Q) baseband inputs. The 3-phase mixer generates I-Q outputs applying the 3 phase clocks from the oscillator. This way both the oscillator and the mixer save power consumption compared to the conventional 4-phase implementation. The quadrature generation method will be explained in more detail in subsection 5.4. As the non-coherent BFSK modulation is used, the RX LO phase does not need to be synchronized with TX, and hence a power hungry PLL can be avoided for LO generation. In this RX a free running oscillator is used, which is periodically corrected by
the ‘frequency correction’ block based on a crystal reference clock (CLKR) to save power consumption drastically. The crystal clock is anyway needed for a precise duty-cycling of the TRX system. The frequency correction is targeted at the starting few phases of the CLKR after the RX is turned ON. As the ON time for a WSNs RX is usually short to save energy, the temperature variations can be small and neglected. If not, the frequency correction block can be periodically enabled and switched off after correction.

5.3.1 Multiple Access Scheme

This receiver is targeted to be used in a synchronized rendezvous transceiver system [53]. In these systems, a time division multiple access (TDMA) scheme is used with the help of an accurate clock. The transceivers are duty-cycled and periodically switched on for a small time (in the range of microseconds) for communication and then switched to sleep mode to reduce energy. Therefore, the same frequency can be used by multiple sensor nodes using a different time slot. Therefore there is only one channel assumed. For WSNs applications the duty-cycle is usually very small and therefore a large number of users can be supported just by TDMA. We exploit this scenario where the local oscillator (LO) does not need to select a channel but only needs to correct its output frequency with respect to the transmitter. Because of no co-channel interferences being present, the phase noise requirement of the LO is relaxed [58].

5.3.2 Modulation

Many low energy receiver architectures are proposed based on envelope detector based OOK modulation, such as in [33]. However, OOK modulation is sensitive to interference present in the operating band. Moreover, a high selectivity band-pass-filter is essential at the receiver front-end before the mixer to prevent large out-of-band blockers to saturate the envelope detector. FSK receivers have better selectivity and out-of-band interference robustness and also have been proposed for ultra low power applications [31, 101]. As mentioned in Chapter 4, binary modulation schemes are suitable for WSNs transceiver as they are simple and low power. Therefore we use BFSK modulation and target to improve the energy-per-bit and in-band interference robustness. We choose non-coherent BFSK modulation because it does not need phase synchronization. The frequency correction block of the LO is switched off after correction and leaves the oscillator free running to save power. Unlike a PLL this free running oscillator can have a LO frequency error and the system has to be robust enough against this. Based on top level simulations, we choose
to use +/- 8 MHz BFSK frequency difference together with 8 MHz of low-pass-filter 3-dB bandwidth considering the trade-off between the bandwidth occupancy and robustness to RX LO frequency error. In the chirped-FSK [48] modulation scheme, a frequency addition of +/- 8 MHz to the instantaneous frequency of the chirped-LO, represents 1/0 data.

![BFSK direct-conversion mixer-first 3-phase receiver architecture.](image)

**Figure 5.3: BFSK direct-conversion mixer-first 3-phase receiver architecture.**

### 5.3.3 Three Stage Ring Oscillator

A ring oscillator is chosen for this receiver because of: 1. the fast turn-on time, which helps to reduce energy consumption for a duty-cycled radio, 2. the low power consumption when the phase noise requirement is moderate or low [102], 3. easy scalability and drastic reduction of power in more advanced CMOS technologies, 4. wide tuning range, suitable for high bandwidth chirped-LO communication, and 5. low area. Although LC oscillators are known to consume less power than ring-oscillators for a given phase noise [103], the LC oscillator startup current is often a limiting factor for ultra low power operation (<100uA) unless large area consuming high Q inductors are used. An on-chip inductor with a moderate Q and inductance values suitable for low-cost WSNs radio limits the power minimization of the LC oscillators.

It has been shown that a three stage ring oscillator consumes less power than a higher number of stages [104]. A four-stage ring oscillator such as in [105], which is suitable for an I-Q direct conversion receiver, usually consumes more power because of extra capacitance of the cross-coupled devices. The power consumption of the 3-stage ring oscillator is less than 3/4 of the 4-stage ring oscillator because the latter needs these extra cross-coupled
devices which are required to avoid undesired states, related to the even number of stages used.

5.3.4 Three Phase to Quadrature Generation

From the three-phase clock, we need to generate I-Q baseband signals for low power BFSK demodulators. The three phase mixer output is combined as shown in Figure 5.4. The three

\[
\begin{align*}
P &= A_0 - A_{240} \\
Q &= A_0 - A_{240} \\
I &= \sqrt{3}A_0 \\
\end{align*}
\]

Figure 5.4: Three-Phase mixer and I-Q generation.

outputs of the mixer can be represented as:

\[
\begin{align*}
A_0 &= A \cos(\omega_{IF}t + \theta_0) \\
A_{120} &= A \cos(\omega_{IF}t + \theta_0 + \frac{2\pi}{3}) \\
A_{240} &= A \cos(\omega_{IF}t + \theta_0 + \frac{4\pi}{3}) \\
\end{align*}
\]

where $\omega_{IF}$ is the IF frequency, $A$ is the signal amplitude after mixer and $\theta_0$ is a initial phase of the incoming RF signal. For BFSK direct-conversion, $\omega_{IF}$ represents the data, by changing between $\Delta f$ (DATA=1) and $-\Delta f$ (DATA=0). Subtracting $A_{120}$ to $A_{240}$. we obtain:

\[
A_{120} - A_{240} = \frac{A}{2} \sin(\omega_{IF}t + \theta_0 + \pi) \sin\left(\frac{\pi}{3}\right) \\
= \sqrt{3}A \sin(\omega_{IF}t + \theta_0)
\]

(5.11)
which produces the quadrature signal with respect to (5.8), however with a gain of $\sqrt{3}$. Any two of the three phases can be subtracted from each other to form a 90 degree phase difference with the other. For simplicity, we show a 50% duty-cycled clock in Figure 5.4. However, the quadrature generation method shown here is still valid for a 3-phase clock with any clock duty-cycle. The power consumption of this extra $\sqrt{3}$ amplification is negligible compared to the oscillator power when added later in the IF path where the noise figure requirement is very relaxed.

### 5.4 Ultra Low Energy Receiver Circuits

In this section, the circuit design and implementation for this chirped-clock ULP receiver is described. The implementation is done in CMOS 65 nm technology.

#### 5.4.1 Three Phase Mixer

The implementation of the 3-phase mixer concept of Figure 5.4 is shown in Figure 5.5. A passive voltage sampling mixer is used because it has higher conversion gain compared to a switching mixer [106], and good linearity and also low power consumption compared to an active mixer [107]. Subtraction of the two phases is done by a differential amplifier. As amplifiers are needed for baseband gain anyway, the quadrature is generated from the 3-phase mixer output without extra power consumption. To match the gain of the I and Q-path, the I-path is designed to have $\sqrt{3}$ times higher gain than the Q-path.

Although there is no static power consumption in a passive voltage sampling mixer, dynamic power is consumed in the oscillator (or in the LO driver) due to the mixer switch gate voltage transitions. In this design, the switch size is chosen considering the trade-off between the noise figure and the power consumption. This resulted in a high mixer switch resistance as the switch device sizes need to be very low to save high frequency switching power. For proper operation of the mixer a $\frac{1}{3}$ duty cycle LO is required so that mixer switches ON time do not overlap [108].

Based on the system optimization in Chapter 2, the targeted noise figure of the receiver is 18 dB. If the noise factor of one mixer switch kernel is $F_{\text{kernel}}$, then the noise factor of the I-path and Q-path of the mixer can be written as:

$$F_{\text{mixI}} = F_{\text{kernel}}, \quad F_{\text{mixQ}} = \frac{2F_{\text{kernel}}}{3}$$  \hspace{1cm} (5.12)

as the noise power is 2 times because of the two path and signal power is 3 times. So, the
Q-path has $10 \cdot \log_{10}\left(\frac{3}{2}\right) = 1.8 \, dB$ less noise figure than the I path. The value of $F_{\text{kernel}}$ depends on the switch resistance, duty cycle and source resistance [109]. The simulated $F_{\text{kernel}}$ in this case is 17 dB (1 dB margin kept from the targeted 18 dB) when the source impedance is 50 Ohm and $R_{SW}$ is about 410 $\Omega$.

![Figure 5.5: Receiver front-end: Input matching, 3-phase mixer and baseband I-Q generation.](image)

### 5.4.2 Input Matching

The input impedance of the 3 phase mixer can be evaluated using N-path filter analysis [110]. Assuming a $\frac{1}{3}$ duty cycled LO, without L-C matching network at the RF input of the receiver, the input impedance for a single-ended 3-phase passive mixer-filter can be derived as:

$$Z_{in} = \frac{R_{SW} + H_n R_S}{1 - H_n} \quad (5.13)$$

where $R_S$ is the source resistance, $R_{SW}$ is the switch ON resistance, $n$ is the number of phases used, =3 in this case, and $H_n(f_S)$ is the transfer function of the passive mixer for the first harmonic of the oscillator frequency from antenna input, $v_{in}$ to mixer core $v_f$ (see Figure 5.6), given by $H_n = \text{sinc}^2\left(\frac{2\pi}{f}\right)$. In this case $Z_{in}$ is much higher than the required 50 $\Omega$. Impedance matching by tuning the resistance in the baseband side of a passive mixer [111]
can not be used in this case as $R_{SW}$ is very large compared to $R_S$. We use an L-C circuit as shown in Figure 5.5 to realize impedance transformation to 50 Ω. The simplified RF input circuit model is shown in Figure 5.6 including bond-wire inductances and pad capacitances included in $L_M$ and $C_M$ respectively. Detailed analysis of the input matching is out of the scope of this thesis. The L-C in resonance was kept at 2.45 GHz and by iterative simulation the input matching at the target frequency was achieved, with $L_M = 9.6$ nH and $C_M = 0.43$ pF. Considering some approximate bond-wire inductance and pad capacitance, we use 7.5 nH of inductance (off-chip) and 0.3 pF of capacitance (on-chip). Another advantage of this matching network is that it produces passive voltage gain from antenna output, $V_{in}$ to the mixer input, $V_m$. The following approximate relation can be used to relate the voltage gain and the quality factor the L match impedance transformation:

$$G_V = \frac{R_P}{R_S \cdot \frac{1}{2Q}}$$

(5.14)

where $R_P$ is the impedance looking into the passive mixer. As the L and C values are chosen by iterative simulation, we obtained the quality factor (Q) and Rp of the matching network by reverse calculation: they are about 2.9 and 450 Ohm respectively. Therefore the voltage gain due to the matching circuit can be calculated by (5.14) and it is 1.5 (4 dB). Approximately 5-6 dB noise figure improvement is observed in simulation due to this L-C circuit. The capacitance $C_M$ (0.43pF) also helps to reduce LO to RF feedthrough as its value is much higher than the parasitic of the small sized mixer switches (<5 fF). Moreover, the L-C filter exhibits low-pass pre-filtering before the mixer thus prevents harmonic down conversion in case there are higher harmonics present in the receiver input.
5.4.3 LO Generation

In this subsection we describe the ring oscillator, digital control of the oscillator, frequency correction method and the chirp generator used in the proposed receiver.

![Three stage ring oscillator with current starved inverters and the generated three phase clock waveform at 2.4 GHz.](image)

Figure 5.7: Three stage ring oscillator with current starved inverters and the generated three phase clock waveform at 2.4 GHz.

5.4.3.1 3-phase ring oscillator

The ring oscillator is implemented by current starved CMOS inverters as shown in Figure 5.7. A single-ended oscillator is chosen over differential implementation as the passive mixer is single-ended. The single-ended mixer is chosen considering receiver power and noise figure tradeoff. The oscillator drives the mixer directly (AC coupled and mixer gates are biased to 0.6V); removing LO driver power consumption. As the phase noise requirement of the oscillator is relaxed for sensor network applications, we use minimum device sizes required by the ring oscillator to drive the mixer load at the highest frequency of operation (2.5 GHz) to minimize power.

Ideally a duty cycle of $\frac{1}{3}$ is required to ensure no overlap of clock phases in the mixer switches. However, a 3-stage n-p balanced (where pMOS device width is increased by the nMOS/pMOS mobility ratio) ring oscillator output clock produces 50% duty cycle. By reducing the pMOS device size in the inverter, the rise time can be increased and thus duty cycle can be reduced slightly to 45%. Less pMOS size also helps to minimize overall capacitance compared to the balanced design. A duty cycle of 45% still causes significant clock overlap, but, does not significantly degrade the passive mixer noise figure. As $R_{SW}$ is
quite high, the time constant $C_M R_{SW}$ is high compared to the overlap time of the switches. That is why there is negligible interaction of charges between the mixer baseband side capacitances. Simulations show that the use of this clock increases the noise figure by $1.5 \, \text{dB}$ and decreases the gain by $1.5 \, \text{dB}$ compared to an ideal $\frac{1}{3}$-phase clock. Simulated phase noise of the oscillator is $-104 \, \text{dBc/Hz}$ at $16 \, \text{MHz}$ offset. This is acceptable because it provides $22 \, \text{dB}$ SNR after the LO mixing due to an interference with $10 \, \text{dB}$ more power than the signal at $16 \, \text{MHz}$ apart from the LO frequency. The interference is considered to be present at $16 \, \text{MHz}$ far from the LO, which is two times the IF filter 3-dB bandwidth of $8 \, \text{MHz}$. The target is to reduce the interference effect due to LO phase noise to a negligible minimum when it is present at two times the bandwidth of the IF filter. This choice of specification helps to have both low LO power and less effect of LO phase noise on the system performance.

5.4.3.2 Digitally Controlled Oscillator (DCO)

A set of parallel current sources and switches is used to control the ring oscillator frequency digitally. The current sources control the ring oscillator current without any extra mirroring to reduce power consumption. The current sources operate in weak inversion to have larger headroom for the oscillator. In total 15 bits are used in the DCO to control the current of the oscillator. Among those, 4 bits are kept for coarse correction for process variation to be done at power-up of the receiver. The other 11 bits are used for fine frequency correction and chirp clock generation described in Subsection-5.4.4. A Frequency Correction Loop (FCL) is used to correct the oscillator frequency. Among the 11 bits, 6 bits control unary current sources and 5 bits control binary current sources. Current mismatch for the sub-threshold region can be approximated as [112]:

$$\frac{\sigma_{\delta I_D}}{I_D} = \frac{A_{VT}}{mV_T \sqrt{WL}}$$

(5.15)

where $W$ and $L$ are the width and length of the device respectively, $V_T$ is the thermal voltage $= kT/q$, $m$ is the sub-threshold slope factor and $A_{VT}$ is the threshold voltage mismatch parameter. Considering the area and accuracy trade-off, the DAC is designed for 9 bits of accuracy. To keep the frequency error less than $1 \, \text{MHz}$, while having a frequency range of $500 \, \text{MHz}$, approximately 9 bit of frequency accuracy is required.
5.4. Ultra Low Energy Receiver Circuits

5.4.3.3 Frequency Correction Loop (FCL)

The RX LO frequency needs to be corrected for process, supply voltage and temperature variations to a value known to both TX and RX. We use the circuit shown in Figure 5.8 to do that. The 4+11-bit code for the required frequency is stored in on-chip registers. The coarse 4-bit correction is targeted to mitigate the process variations. Supply and temperature variations are corrected by the 11-bit code each time the receiver switches on. When the frequency correction is done, the FCL is switched off to save power. As the switch-ON time of the receiver is short, temperature changes within that time are not expected to be significant. The oscillator PSRR is made good enough to avoid significant phase noise spur due to the dynamic power supply variation. A PSRR of 20dB is good enough to reduce the frequency deviation to less than 0.5 MHz assuming 10 mV maximum ripple in the supply.

The frequency correction procedure is as follows. In this case, switch S2 is closed and S1 is open. The frequency from the oscillator triggers a counter which counts the number of positive edges of the LO clock in 1 µs, half a period of CLKF. This clock frequency is 0.5 MHz, generated by frequency division of 64 MHz CLKR input which is assumed

Figure 5.8: DCO and frequency correction circuit. Switch S1 is open and S2 is closed for frequency correction.
to be coming from a crystal oscillator. The requirement of 64 MHz came from the BFSK
demodulator working at 8 Mbps. For a 2.4 GHz LO frequency, the counter output should be
2400. If this is not the case, the counter output is subtracted from 2400. This subtract output
is the indication of the frequency error. It must be multiplied by the DCO MHz/code ratio
\(K_D\) to convert it from a frequency value to the required code to be added. An 11 bit adder
(A2) adds this multiplied value to the previously stored value in register R2. The default
scaled factor used here is 4 because it increases the DCO output by 1 MHz (note that the
counting time is \(1 \mu s\)) at the nominal condition. A power of 2 is used in the multiplication
so that it can be done by just bit shifting without consuming any power. Although \(K_D\)
changes with PVT variation, the frequency loop can repeat its operation to get the required
frequency accuracy.

The power consumption of the FCL is dominated by the counter which counts the
number of edges of the LO. Other blocks operate in 0.5 MHz, thus have much less power
than the counter. To optimize the counter power consumption, we use 12 divide-by-2
circuits to realize the 12 bit counter. The first 6 dividers, which are operating at higher
frequency, are implemented by True Single Phase Clocking (TSPC) flipflops. The rest of
the dividers are realized by static CMOS flipflops as they operate at lower frequencies.

5.4.4 Chirp Clock Generation

The oscillator frequency is chirped by sweeping the bias current of the ring oscillator.
Although the ring oscillator shows a quite linear frequency with respect to the bias current,
the non-linearity increases with increasing chirp bandwidth. The simulated frequency errors
are shown in Table 5.1. From the BER simulation, we see (Section 5.5) that a frequency
error of maximum 2 MHz is acceptable. Both RX and TX need chirped-LO with ideally
the same characteristics; starting frequency \(f_S\), chirp time \(T_{CH}\) (or bandwidth) and
frequency-time slope \(\beta\). The starting frequency is determined by the FCL block. By
using a crystal oscillator, the chirp time for both TX and RX is fixed. The last part is to
match the \(\beta\) for both TX and RX; this is discussed in this subsection (to a value known to
both TX and RX).

The DCO is controlled digitally to generate the required chirped clock. Figure 5.9
shows the complete chirp generation circuit block diagram. Some parts of the FCL and
DCO are shown to illustrate the chirp generator interfaces. To generate the up-chirp, a
digital ramp generator is used. It increases the DCO current over a specified value given by
the frequency correction loop. It consists of an 11 bit register (R3) and an 11 bit adder (A3)
and clocked by the external 64 MHz clock signal. Ramp generator output data \(D_{CH}\) enters
Table 5.1: Simulated oscillator linearity error

<table>
<thead>
<tr>
<th>Freq. range (GHz)</th>
<th>Bandwidth (MHz)</th>
<th>Max. error freq. (+/-) (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.4 to 2.45</td>
<td>50</td>
<td>0.43</td>
</tr>
<tr>
<td>2.4 to 2.5</td>
<td>100</td>
<td>0.55</td>
</tr>
<tr>
<td>2.32 to 2.5</td>
<td>180</td>
<td>0.85</td>
</tr>
<tr>
<td>2.2 to 2.55</td>
<td>360</td>
<td>2.2</td>
</tr>
<tr>
<td>2 to 2.5</td>
<td>500</td>
<td>5.2</td>
</tr>
<tr>
<td>1.5 to 3</td>
<td>1500</td>
<td>41</td>
</tr>
</tbody>
</table>

to the FCL to control the DCO through an adder. A control circuit generates the 1 MHz clock with short pulses from the 64 MHz clock to reset the register R3 periodically. This clock determines the chirp time, which for our specific case equals 1 µs.

The chirp slope is controlled by the slope corrector block. As the slope changes with process variation, a correction cycle is used before the communication starts. The slope corrector consists of a register R4, a subtracter and a divider. It interacts with the FCL register R2 to calculate the slope. To generate a 2.4 GHz to 2.5 GHz chirp, the following steps are used. First the FCL corrects the oscillator required frequency to 2.5 GHz, then the corresponding 11 bit code for 2.5 GHz is transferred from R2 to register R4. Next the FCL is activated again to correct the required oscillator frequency to 2.4 GHz. Now, registers R2 and R4 contain the digital codes corresponding to 2.4 and 2.5 GHz respectively. The subtracter gives the difference of these codes, this difference is divided by 64 (As the ramp generator clock frequency is 64 times its reset frequency) by bit shifting. The divider output code is fed to the adder A3 to control the increments of the ramp generator. The quantization error due to the use of a digital code is 0.5 LSB = 0.5(100/64)=0.78 MHz. However, the effect of this error on the communication is negligible because the frequency error averages out during a bit period. The chirp generation block consumes 8.4 µW of power from the 1.2 V supply.

5.4.5 IF Amplifiers

The IF path of the receiver, shown in Figure 5.10, consists of four amplifying and filtering stages for both I and Q. Open loop differential amplifiers are used to produce gain at low power. The impedance of the mixer output is different for the I and Q paths because of its asymmetric mixer structure. Because of this, the output spectrum and the noise figure is different for the I and Q paths. However, thanks to the simple binary modulation
and the zero crossing demodulator, the receiver performance is not sensitive to these I-Q mismatches. The resistive load of each differential amplifier provides bias for the subsequent stage. The input transistors of the differential amplifier are kept in sub-threshold to get maximum $g_m$ for a given bias current. Alternate stages of the differential amplifier are realized as split-source-capacitive-coupled differential amplifiers [32] which reduce the low frequency gain to reject offset and flicker noise amplification. Because of the finite output resistance $r_b$ of the tail current source the maximum attenuation at very low frequencies is limited to $(1 + g_m r_b)$, which is roughly -5 dB per stage. The high-pass filter 3 dB bandwidth is set at 700 kHz with $C_S = 5$ pF. The bias current of the amplifiers is scaled down along the chain to achieve minimum power for a given noise figure. Each amplifier stage produces 13-15 dB gain and one-pole low pass filtering. The poles are created only by parasitic capacitance so that minimum bias current can be used in the amplifiers. The overall 3 dB cut-off frequency for the 5-pole IF system is at 8 MHz. Total gain is approximately 57 dB. The total power consumption of I and Q path together is 67 $\mu$W in 65 nm CMOS. The I-path gain is increased by $\sqrt{3}$ times more than the Q path to match the gain, as shown in

Figure 5.9: Chirp clock generation circuit block diagram. Switch S2 is open and S1 is closed for chirp clock generation.
5.4. Ultra Low Energy Receiver Circuits

Figure 5.10: IF amplifiers of the receiver.

Figure 5.11. As the I-Q matching requirement of the demodulator is quiet relaxed and only affect the required demodulator SNR, exact factor of $\sqrt{3}$ is not necessary. The gain ratio is achieved by component sizing. From (5.12), we see that in the mixer stage, the I path noise figure is 1.8 dB higher than in the Q path. Also, the lower gain of the I path mixer section is compensated in the IF amplifier, adding additional noise. Including both mixer and IF amplifiers, the simulated noise figures of the I and Q path are shown in Figure 5.12. The noise figure of the Q-path is better by 4 dB compared to the I-path.

5.4.6 Low Power BFSK Demodulator

For the direct conversion BFSK receiver, demodulation can be performed by just one flipflop [113], after hard limiting the I and Q baseband outputs. After down conversion, positive and negative frequencies represent ’1’ and ’0’ data and those can be extracted by the flipflop that detects phase reversals as explained in [113]. For a single flipflop demodulator, any missing edge in the I or Q path can cause an error. To improve, we modify this demodulator by combining all the possible edges from both the positive and negative transition from the I and Q-path. The demodulator block diagram and the circuits are shown in Figure 5.13. Among these outputs only the last valid edge is chosen because the initial edges are more inter-symbol interference affected. This modification improves
the BER performance for a given SNR without increasing the power consumption much. BER analysis for the demodulator and simulations are separately described in the next Section.

The limiter in the I and Q-path is realized by a low power comparator [114] clocked by a 64 MHz input clock to achieve a datarate of 8 Mbps. The comparator output is latched by a set of True Single Phase Clocked (TSPC) flipflops which consume less power than conventional CMOS flipflops. To reduce the power consumption, four flip-flops are combined into one transmission gate latch. Any of the four inputs of the latch (I, IB, Q, QB) can overwrite the previous input and thereby the last edge of any four possible combinations comes out at the output. In this way four flipflop combinations can be achieved only consuming the power of one flipflop. Finally the output data is latched by a static CMOS flipflop. The comparators consume $5.2 \mu W$ and rest of the demodulator power equals $1 \mu W$ at 1.2 V power supply.

### 5.5 BER Simulation of the Receiver

In this section, we discuss the simulation of the BER performance of the demodulator as a function of the SNR at the input of the demodulator. The BER-SNR relation will provide the SNR required for the required BER ($10^{-3}$), that will help us to estimate the receiver sensitivity and also to model chirped-clock communication BER with respect to noise and interference.
5.5. BER Simulation of the Receiver

5.5.1 Demodulator BER Simulation Result

We modeled the system in MATLAB. Real valued white Gaussian noise is added to the FSK modulated signal before feeding it into the receiver. Simulations are done for 204800 bits. Five stages of first order low-pass filtering and two stages of first order high pass filtering are modeled in the IF path. The comparison between the ideal theoretical non-coherent BFSK detector and the proposed detector and filtering is shown in Figure 5.14 by BER simulation. The simulation conditions are listed in Table 5.2. The receiver sensitivity can be calculated by the following relation:

\[
P_{\text{Sensitivity}} = -174 + NF + 10 \log(BW) + SNR
\]  

Figure 5.12: Simulated overall receiver noise figure of I and Q path with respect to IF frequency.

<table>
<thead>
<tr>
<th><strong>Parameters</strong></th>
<th><strong>Values</strong></th>
<th><strong>Unit</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>Carrier Frequency</td>
<td>2.45</td>
<td>GHz</td>
</tr>
<tr>
<td>Bit/data rate</td>
<td>8</td>
<td>Mbps</td>
</tr>
<tr>
<td>Frequency separation</td>
<td>+/- 8MHz</td>
<td>MHz</td>
</tr>
<tr>
<td>Simulation Sampling Frequency</td>
<td>10</td>
<td>GHz</td>
</tr>
<tr>
<td>LPF cutoff</td>
<td>8</td>
<td>MHz</td>
</tr>
<tr>
<td>LPF order</td>
<td>5</td>
<td>-</td>
</tr>
<tr>
<td>HPF cutoff</td>
<td>700</td>
<td>KHz</td>
</tr>
<tr>
<td>HPF order</td>
<td>2</td>
<td>-</td>
</tr>
</tbody>
</table>
where $NF$ is the noise figure of the receiver front end and $SNR$ is the signal to noise ratio required by the demodulator for the given BER. From the simulation we see that for a BER of $10^{-3}$ the demodulator needs 15 dB of SNR. So, for bandwidth $BW = 8$ MHz and $NF = 18$ dB (average of I and Q-path), we get a sensitivity of -71 dBm.

### 5.5.2 BER Simulations of the Chirped-Clock Receiver

To determine the BER of the receiver with and without chirped communication, we simulated the BER for the chirped and non-chirped system, modeled in MATLAB. The simulated BER for a Single Tone Interferer (STI) with frequency sweep of the interferer near the carrier frequency is shown in Figure 5.15. The simulated BER for STI near to the carrier frequency for different SIR is shown in Figure 5.16. As we can see there is a significant reduction of BER due to the use of the chirped clock signal. In Figure 5.15,
5.5. BER Simulation of the Receiver

The $n_b$ is larger, therefore the BER for chirped-LO, according to (5.7), is reduced by an averaging phenomenon of the non-chirped BER. However, there was no definitive explanation found for the ‘oscillation’ of the BER at higher frequencies. For Figure 5.15, the average BER at 3 dB SNR for the chirped-LO case is approximately 0.02 ($n_b=16$), which is close to the value of Figure 5.16 for $n_b=8$.

The SIR requirement to achieve a BER of $10^{-3}$ is 6 dB for $n_b=8$ and 2 dB for $n_b=1$ at 100 MHz of chirp bandwidth. To compare this 4 dB advantage from $n_b=8$ to $n_b=1$, using (5.6) and (5.7) we assume that $n_b=8$ can be considered as a large value because here $b_{CH}=12.5$MHz is less than $2 \cdot f_{lf} = 16$ MHz. The corresponding SIR advantage is 6.3 dB using $n_b=1$ compared to a large $n_b$ value for this ideal non-coherent receiver of Figure 5.2. The robustness against interference increases when a higher chirp bandwidth is used. For example when the chirp bandwidth is 360 MHz, and only one bit is used in one chirp ($n_b=1$), the SIR requirement according to the simulation is -12 dB to achieve a BER of $10^{-3}$.

For $n_b=1$, the SIR advantage of using a chirp compared with the non-chirped communication for a given BER is $\frac{B_{CH}}{2 \cdot f_{lf}}$ according to (5.6). Using this and with $f_{lf}=8$MHz, $B_{CH}=100$MHz has advantage of about 8 dB and $B_{CH}=360$MHz has advantage about 13.5dB. In corresponding simulation the SIR advantage for 100MHz and 360MHz are 5dB and 19dB respectively. Therefore the simulation result of 100 MHz is worse and 360MHz is better than the modeled equation. Obviously, there is some discrepancy expected due to the difference in implemented IF filter and demodulators characteristics and also due to the fact that the spread-ed interference is assumed like white noise. There

Figure 5.14: Simulated BER of the receiver in channel noise; compared with ideal non-coherent FSK receiver.
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Figure 5.15: Single tone interference response at different interfering frequencies; SIR = 3 dB; with and without chirped LO. Here $n_b=16$ and $B_{CH}=100$MHz.

could be some potential cancellation of correlated interference between I and Q path which leads to better simulation result in-case of 360MHz. However, contributions of these are discrepancy sources are not investigated further.

5.5.3 SNR Degradation Due to Frequency Error

In chirped clock communication, matching of the TX and RX LO frequency w.r.t time is very important. If the clocks are matched, the performance of the chirped communication will be as expected. However, there are some sources of frequency errors due to the following imperfections:

1. LO inaccuracy
2. Oscillator frequency-bias current non-linearity.
3. DCO DAC non linearity due to mismatch. (Random)
4. Imperfect chirp synchronization. (Fixed offset)
5. DCO quantization error. (Variable)

To predict the chirped clock communication performance in the presence of clock mismatch offset between the TX and the RX, we simulated the RX demodulation performance in the presence of frequency offsets. A fixed frequency offset in the LO is provided in the non-chirped transceiver. MATLAB BER simulation results with LO frequency offsets are
Figure 5.16: Single tone interference response at different interfering power; \( n_b = 1 \) and \( n_b = 8 \), same datarate of 8 Mbps. The interference frequency is at 5 MHz far from the LO frequency.

shown in Figure 5.17. When exactly 2 MHz offset is used, the BER is better than 1 MHz offset at high SNR levels. This is because of periodic carrier and LO phase synchronization. We therefore simulated with an frequency offset close to 2 MHz but not exactly 2 MHz so that the carrier and LO phase is aligned almost never. Similar approach is taken for other offsets also. Simulations show an SNR degradation of about 3 dB for BER of \( 10^{-3} \) when the frequency error is 2 MHz. The target is to limit the frequency error within 2 MHz.

5.6 Full Chip Integration

The complete test chip block diagram is shown in Figure 5.18. The RF input is R-C filtered and used in the first differential amplifier of the I-path as a reference voltage. IF path outputs (comparator inputs) are separately amplified to the output for noise figure measurements for both the I and Q-paths. An external 64 MHz clock is used in the chirp generator, in the demodulator and to generate the following clocks:

1. 8 MHz for data sampling (bit clock) and TX modulation
2. 1 MHz for the chirp period (8 bits in one up-chirp)
3. 0.5 MHz for the frequency counter in the FCL
4. 0.5 MHz for the control signals of the slope corrector.
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Figure 5.17: BER versus SNR of the system with LO frequency offset.

Table 5.3: Simulated power consumption of receiver blocks

<table>
<thead>
<tr>
<th>Block</th>
<th>Power Consumption (µW)</th>
<th>Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Oscillator</td>
<td>95</td>
<td>46%</td>
</tr>
<tr>
<td>IF amplifiers (I+Q)</td>
<td>67</td>
<td>33%</td>
</tr>
<tr>
<td>Demodulator</td>
<td>6.2</td>
<td>3%</td>
</tr>
<tr>
<td>FCL</td>
<td>22</td>
<td>11%</td>
</tr>
<tr>
<td>Chirp Generator</td>
<td>8.4</td>
<td>4%</td>
</tr>
<tr>
<td>Control circuits</td>
<td>6</td>
<td>3%</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>205</strong></td>
<td><strong>100%</strong></td>
</tr>
</tbody>
</table>

A separate DCO with amplifier/driver is used (bottom part of the figure) such that each IC can serve as a TX as well. The TX can generate both FSK and chirped-FSK modulated signals. In this way the overall transceiver BER can be measured for both FSK and chirped-FSK communication. Modulation is done by controlling the DCO current similar to chirp generation. A separate 4-bit DAC is used in the TX DCO to control the BFSK frequency separation. The DAC input is controlled by the slope generator in the chirp generation block, therefore the same process information can be used to calibrate and get the required frequency separation of the FSK modulated signal. The RX operates at 1.2 V supply voltage.

Two external components are required for the receiver: 1) An inductor, used for input matching, occupying a board area of $1.12\text{mm} \times 0.7\text{mm} \approx 0.8\text{mm}^2$. 2) A crystal oscillator,
5.7 Measurement Results

The receiver is fabricated in a 65 nm CMOS process of ST Microelectronics. The chip micro-graph is shown in Figure 5.19. The total die area is 1.4 mm x 1.4 mm and it is packaged in a QFN36 package. The packaged device is mounted on a PCB to measure the IC performance. The area occupied by the RX and the DCO, as marked in the figure,
Chapter 5. Ultra Low Power/Energy Interference Robust Receiver IC Implementation and Measurement Results

Figure 5.19: Chip Micrograph (1.4x1.4\textit{mm}^2 in 65nm CMOS).

Figure 5.20: BER Measurement setup with RX and TX PCBs
are 0.07 mm$^2$ and 0.04 mm$^2$ respectively.

### 5.7.1 Measurement of Nonchirp RX

First the non-chirped RX performance is measured after frequency correction of the LO. Unfortunately there is an error in the state machine of the on-chip frequency correction such that it cannot work automatically. It does adjust the frequency in the right direction and with the correct step size, but it requires an external RESET input after each iteration. An improved state machine would only take minor adjustments in the low frequency (1MHz)
control part. For the following measurements, we therefore applied the frequency control code externally. Please note that the parts of the FCL that dominate its power consumption are implemented on-chip in this design. Moreover, the FCL is switched off in operating mode and therefore the energy consumption and interference robustness of the receiver are not affected.

The measured $S_{11}$ of the Ultra Low Energy receiver (ULERX) is shown in Figure 5.21 for LO frequency of 2.4 GHz. It is less then -10 dB from 2 GHz to 2.5 GHz. The measured noise figures of the I and Q paths are shown in Figure 5.22 and compared with the simulations. As we expected, the Q path has a better noise figure then the I path, although there is no clear explanation for the higher than expected noise in the Q-path from 2-7MHz. The FSK tones are at 8 MHz of IF/baseband frequency. However, the oscillator frequency errors can change this by +/- 2 MHz.” The BER of the ULERX is measured for

![Figure 5.23: Measured BER vs. input power of non-chirped ULERX, datarate=8 MHz, $F_{LO}=2.4$ GHz, TX sends a modulated signal $F_{LO} + 8$ MHz or $F_{LO} - 8$ MHz for data=1 and data=0 respectively.](image)

the communication between the on-chip TX and RX. Two separate PCBs with separate ICs are used for TX and RX. The BER measurement setup is shown in Figure 5.20. The TX output power is at -6 dBm, attenuators are placed between TX and RX input to model a wireless channel. The measured BER with changing input power is shown in Figure 5.23. The BER is less then $10^{-3}$ at input power levels of -70 dBm to -35 dBm resulting in a 35 dB of acceptable input power range at one IF path gain setting. The DC component at the IF
due to LO to RF feed-through does not create a problem as the measured BER is as expected.

The effect of the interference power on the receiver depends on the frequency of the interferer. If the interferer frequency is close to the BFSK tones, the receiver is highly affected as shown in Figure 5.24. At least 6-7 dB of SIR is required to achieve a BER of $10^{-3}$. Measured receiver power consumption when operating at 2.4 GHz and the FCL is disabled is 219 $\mu$W. There is an extra 22 $\mu$W when the FCL is activated.

### 5.7.2 Measurement of Chirped LO RX

The chirp generator is activated to do measurements on the Chirped ULERX (CULERX). From the static characteristics of the chirp clock, the maximum error for 100 MHz and 350 MHz bandwidth is 1.4 MHz and 4 MHz respectively, and the average frequency error is 0.45 MHz and 1.3 MHz respectively. With a synchronized chirp LO in TX and RX, the BER of the output data is measured and shown in Figure 5.25. There is a degradation of sensitivity about 3-4 dB at $BER = 10^{-3}$ level because of the above mentioned chirp mismatches. When the clock is chirped from 2.4 to 2.5 GHz the power consumption is 235 $\mu$W (FCL deactivated).

The interference effects on the CULERX were also examined. Figure 5.26 shows the SIR robustness for a BER of $10^{-3}$ at different interferer offset frequencies. The single-tone

---

**Figure 5.24**: Measured SIR required to achieve a BER of $10^{-3}$ in non-chirped ULERX at different $\Delta f$ where one interfering tones is present at $f_{LO} + \Delta f$, data rate = 8 Mbps. Similar results are found when $\Delta f$ is negative.
interference at different frequencies in the band has similar effects throughout the chirped bandwidth. Therefore, the communication is not interrupted by interference whatever is the interferer location as shown in the figure. Comparatively higher input power is given to the receiver to make sure noise does not have any significant effect. The worst case performance of CULERX across frequency range is indicated by $SIR_{MIN}$. At lower value of chirp bandwidth, almost there is no improvement, but at higher chirp bandwidth $SIR_{MIN}$ improves up-to 15 dB over ULERX. Also, Table 5.4 shows the performance of the CULERX at different chirp bandwidths and data-rates, also compared to ULERX (row1). Best robustness is achieved when the chirp bandwidth is 360 MHz, however at a reduced data rate of 1 Mbps ($n_b = 1$). A higher chirp bandwidth affects the sensitivity significantly because of the large absolute frequency error. When the number of bits in a chirp is 1, the robustness is better. However, it limits the data-rate and energy efficiency.

The BER at different SIR is shown in Figure 5.27 to compare CULERX performance at different BERs. For $BER=10^{-3}$, CULERX has up-to 12 dB more interference robustness compared to an ideal non-coherent receiver. The advantage increases for lower BER and reduces at higher BER. Also a steeper BER reduction can be observed with respect to SIR when $n_b$ is reduces from 8 to 1 or 2.

Table 5.5 compares the performance of the CULERX with recently reported ultra low power/energy receivers. Unchirped, the maximum energy efficiency achieved by the receiver is three times better than the highest performance reported (row 1). Chirped, the
5.8 Conclusion

Table 5.4: Performance summary of the chirped clock receiver (CULERX)

<table>
<thead>
<tr>
<th>Data rate</th>
<th>Chirp Bandwidth</th>
<th>( f_S )</th>
<th>Chirp time</th>
<th>bits in a chirp ((n_b))</th>
<th>Sensitivity</th>
<th>( SIR_{MIN} ) ¹</th>
<th>Time Band-width Product</th>
<th>Power consumption</th>
<th>Energy</th>
</tr>
</thead>
<tbody>
<tr>
<td>8 (ULERX)</td>
<td>0</td>
<td>2.4</td>
<td>N/A</td>
<td>N/A</td>
<td>-70</td>
<td>7</td>
<td>N/A</td>
<td>219</td>
<td>27</td>
</tr>
<tr>
<td>8</td>
<td>100</td>
<td>2.4</td>
<td>1</td>
<td>8</td>
<td>-66</td>
<td>7</td>
<td>100</td>
<td>235</td>
<td>29</td>
</tr>
<tr>
<td>4</td>
<td>100</td>
<td>2.4</td>
<td>1</td>
<td>4</td>
<td>-69</td>
<td>6</td>
<td>100</td>
<td>235</td>
<td>58</td>
</tr>
<tr>
<td>2</td>
<td>100</td>
<td>2.4</td>
<td>1</td>
<td>2</td>
<td>-69.5</td>
<td>6</td>
<td>100</td>
<td>235</td>
<td>116</td>
</tr>
<tr>
<td>4</td>
<td>90</td>
<td>2.4</td>
<td>0.25</td>
<td>1</td>
<td>-71</td>
<td>2</td>
<td>22.5</td>
<td>235</td>
<td>54</td>
</tr>
<tr>
<td>2</td>
<td>180</td>
<td>2.3</td>
<td>0.5</td>
<td>1</td>
<td>-70</td>
<td>-1.5</td>
<td>90</td>
<td>224</td>
<td>108</td>
</tr>
<tr>
<td>1</td>
<td>360</td>
<td>2.15</td>
<td>0.5</td>
<td>1</td>
<td>-66</td>
<td>-8</td>
<td>360</td>
<td>217</td>
<td>217</td>
</tr>
</tbody>
</table>

¹ Minimum SIR required to achieve \( BER = 10^{-3} \), across all interferer frequencies

Table 5.5: Receiver Performance Summary and Comparison (ULERX and CULERX)

<table>
<thead>
<tr>
<th>Author [Ref]</th>
<th>Technology</th>
<th>Power Supply</th>
<th>Frequency</th>
<th>Data-rate</th>
<th>Sensitivity</th>
<th>Power</th>
<th>Modulation</th>
<th>Area</th>
<th>( SIR_{MIN} )</th>
<th>Energy Efficiency</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Unit -&gt;</td>
<td>nm</td>
<td>V</td>
<td>MHz</td>
<td>Kbps</td>
<td>dBm</td>
<td>( \mu W )</td>
<td>mm²</td>
<td>dB</td>
<td>pJ/bit</td>
</tr>
<tr>
<td>This work, nonchirped</td>
<td>65</td>
<td>1.2</td>
<td>2400</td>
<td>8000</td>
<td>-70</td>
<td>219</td>
<td>FSK</td>
<td>0.11</td>
<td>7</td>
<td>27</td>
</tr>
<tr>
<td>This work, chirped</td>
<td>65</td>
<td>1.2</td>
<td>2400</td>
<td>1000</td>
<td>-70</td>
<td>235</td>
<td>FSK</td>
<td>0.11</td>
<td>-8</td>
<td>232</td>
</tr>
<tr>
<td>Huang, [29]</td>
<td>90</td>
<td>1.2</td>
<td>915</td>
<td>10</td>
<td>-83</td>
<td>121</td>
<td>OOK</td>
<td>1.27</td>
<td>5.5</td>
<td>1200</td>
</tr>
<tr>
<td>Bae, [28]</td>
<td>180</td>
<td>0.7</td>
<td>920</td>
<td>5000</td>
<td>-73</td>
<td>420</td>
<td>FSK</td>
<td>-</td>
<td>-</td>
<td>84</td>
</tr>
<tr>
<td>Cook, [31]</td>
<td>130</td>
<td>0.4</td>
<td>2400</td>
<td>500</td>
<td>-100</td>
<td>130</td>
<td>FSK</td>
<td>-</td>
<td>-</td>
<td>1100</td>
</tr>
<tr>
<td>Fletcher, [32]</td>
<td>90</td>
<td>0.5</td>
<td>2000</td>
<td>100</td>
<td>-72</td>
<td>52</td>
<td>OOK</td>
<td>0.1</td>
<td>-</td>
<td>500</td>
</tr>
<tr>
<td>Daly, [33]</td>
<td>180</td>
<td>0.5</td>
<td>2000</td>
<td>100</td>
<td>-65</td>
<td>2500</td>
<td>OOK</td>
<td>0.27</td>
<td>-</td>
<td>2500</td>
</tr>
<tr>
<td>Pandey, [34]</td>
<td>130</td>
<td>1</td>
<td>400</td>
<td>200</td>
<td>-70</td>
<td>44</td>
<td>FSK</td>
<td>0.5</td>
<td>-</td>
<td>220</td>
</tr>
<tr>
<td>D Ye[98]</td>
<td>65</td>
<td>1</td>
<td>915</td>
<td>10</td>
<td>-70</td>
<td>150</td>
<td>Transmit reference</td>
<td>0.225</td>
<td>-7</td>
<td>15000</td>
</tr>
<tr>
<td>Moszzeni, [35]</td>
<td>130</td>
<td>1/0.5</td>
<td>915</td>
<td>200</td>
<td>-75</td>
<td>22.9</td>
<td>OOK</td>
<td>0.2</td>
<td>-</td>
<td>110</td>
</tr>
<tr>
<td>Bae, [36]</td>
<td>180</td>
<td>0.7</td>
<td>80</td>
<td>312</td>
<td>-62</td>
<td>45</td>
<td>FSK</td>
<td>1</td>
<td>-</td>
<td>140</td>
</tr>
<tr>
<td>Zgaren, [37]</td>
<td>130</td>
<td>1.2</td>
<td>902-928</td>
<td>8000</td>
<td>-78</td>
<td>639</td>
<td>FSK</td>
<td>0.49</td>
<td>-</td>
<td>80</td>
</tr>
</tbody>
</table>

receiver can achieve a BER of \( 10^{-3} \) at SIR of -8 dB, at 1 Mbps resulting in a 13.5 dB higher robustness than the previously achieved result in ultra low energy (row 2).

5.8 Conclusion

In this chapter an in-band interference robust scheme is proposed and implemented in an energy efficient BFSK receiver chip in 65 CMOS [49]. A 3-phase direct conversion receiver architecture along with a low power demodulator helps to reduce the power consumption to 219 \( \mu W \) from a 1.2 V power supply outputting data at a 8 Mbps rate. The
receiver achieves a sensitivity of -70 dBm within the 2.4 to 2.5 GHz ISM band. Hence it achieves an energy efficiency of 27 pJ/bit, approximately three times better than recently reported results. Although in the ISM band the maximum allowed bandwidth is 100MHz, a higher bandwidth is used to show the improvement of using chirped-LO. In the chirp-clock communication mode, using a chirp spread of 360 MHz, the receiver can achieve a $10^{-3}$ BER at an SIR of -8 dB across the whole frequency range with only 15 $\mu$W of extra power and a sensitivity degradation of about 4 dB. The robustness is 13.5 dB higher than previously reported literature interference robustness except in [98], where the energy per bit is as high as 15 nJ/bit. Unlike most of the reported receivers, the proposed receiver includes demodulators on-chip and uses the 2.4 GHz band considering antenna size. The receiver uses more switching logics, such as in passive mixer, ring-oscillator, demodulator to be technology scaling friendly. Using a more linear LO generator which supports a wider-band
Figure 5.27: BER change with respect to SIR, where the interfering tone frequency is at the worst possible scenario. For the non-coherent and ULERX, the interferer is at the top of the carrier frequency, for the CULERX, the interferer is at the center of the chirped bandwidth. Chirp has the potential to improve both interference robustness and data-rate further.
Chapter 6

Conclusions

In this chapter, the most important conclusions presented in this thesis are summarized, followed by a presentation of the original contributions. Finally, recommendations for future work are discussed.

6.1 Conclusions

This thesis is targeted towards a Ultra low energy and interference robust transceiver design. More focus is given to the receiver circuits as it is the most critical part of the transceiver for both power consumption and interference robustness.

To minimize the overall transceiver energy of a duty-cycled transceiver, an optimization method is proposed where some key transceiver parameters such as the noise figure and the datarate are chosen optimally (Chapter 2). In this method, two existing energy optimization methods are combined. Comparisons show that the transceiver energy can be reduced by 30 to 60% using this method compared to other conventional approaches. Moreover, this optimization technique is applied successfully in a wakeup radio with a slot based MAC protocol, and optimum parameters for minimum energy are derived.

Quadrature dividers are often used in receiver clock generation and their power consumption can be a significant part of the overall receiver power. To reduce the power consumption of these dividers, a comparison is performed between two important types of flipflops, DTG and CML, for frequency dividers based on their power-jitter product performance (Chapter 3). The dynamic transmission gate logic, i.e. DTGL is chosen for this comparison because it achieves the best power-jitter performance among several flipflop logic families and current mode logic, i.e. CML is chosen because it is the most commonly used in high frequency dividers. Analytical comparison between DTGL and CML flipflops quadrature dividers based on their power-jitter performance is done. The comparison shows
that the DTGL flipflop is one order of magnitude better than CML around 1 GHz of output frequency in 90nm CMOS technology. Its benefit increases further with the reduction of the frequency of operation and also with the technology feature size.

To improve the interference robustness, a chirped-LO based modulation scheme is proposed for FSK and PSK systems (Chapter 4). A simplified analysis shows that the BER of the chirped-LO system is up to ten times better than the corresponding non-chirped system when the narrow-band interference frequency is close to the carrier frequency. The interference robustness of the chirped-LO system is independent of the interference frequency location. Simulation results confirm the simple analysis.

A simplified BER analysis of a chirped-LO direct conversion receiver shows that a higher chirp bandwidth and a low number of bits in one chirp increases the interference robustness (Chapter 5). A new 3-phase direct conversion receiver architecture along with a low-power demodulator is proposed to achieve ultra low energy operation. The fabricated receiver is able to achieve power consumption of 219 $\mu$W from a 1.2 V power supply operating at a datarate of 8 Mbps (datarate during its ON time) in 65 nm CMOS technology. The receiver achieves a sensitivity of -70 dBm within the 2.4 to 2.5 GHz ISM band. Hence it achieves an energy efficiency of 27 pJ/bit, three times better than the state-of-the-art. In the chirped-LO mode, using a chirp spread bandwidth of 360 MHz, the receiver can achieve a $10^{-3}$ BER at an ISR of 8 dB across the whole frequency range with only 15 $\mu$W of extra power and a sensitivity degradation of about 4 dB. The robustness is 13.5 dB higher than previously reported interference robustness of ultra low power/energy receivers. The high robustness achieved here needed higher bandwidth than that allowed in the 2.4 GHz ISM band.

The results obtained in this thesis are benchmarked with other ultra low power receivers irrespective of the implementation, but not with other spread spectrum implementations which are not targeted for ultra low power. This is because this receiver is aggressively optimized for energy consumption at the cost of bandwidth, number of users, number of channels etc. Hence the advantages around chirped-LO communication claimed here are valid within the boundary of ultra low power/energy applications only.

The ultra-low energy techniques that are proposed and validated here can be incorporated in WSNs radios to improve the battery life time of a TRX in a sensor node up to three times. The interference robustness technique proposed here can be used to improve the robustness of a wireless sensor network by more than ten times co-existing with other communication standards.
6.2 Original Contributions

This thesis presents the following original contributions:

1. The system-circuit combined energy optimization of a duty-cycled transceiver system which results in reduced energy consumption by targeting the receiver noise figure and data-rate for minimum energy, depending on the specification, application, device technology and circuit topology specific parameters (Chapter 2).

2. The analytic comparison of flipflop logic families to determine the low power divider topology for a given phase error or jitter performance (Chapter 3).

3. A chirped-LO transceiver system to achieve in-band interference robustness. Simplified BER analysis to assess the chirped-LO system performance (Chapter 4).

4. The three-phase quadrature receiver front-end to reduce the local oscillator and the mixer power consumption (Chapter 5).

5. The flipflop BFSK demodulator suitable for ultra low power operation without sacrificing SNR (Chapter 5).

6. The implementation of a low energy chirped-LO receiver which shows 13-14 dB improvement of interference robustness at ultra low energy (Chapter 5).

6.3 Recommendations and Future Research

Although this work shows good energy and interference robustness performance in silicon, there are several areas suitable for future research to improve transceiver performance further. Some of those areas have potential to improve in both energy and robustness and some have potential to explore new insights and ideas in the proposed system. My recommendations for future work are:

1. **Implementation of low-power chirped-LO synchronization:** In this thesis a chirped-LO synchronization scheme is proposed in appendix B suitable for a low power system. Detailed analysis and implementation of this synchronization method targeted for an ultra low energy transceiver can be a next step. A synchronized chirped-LO of the proposed system has the potential to help in symbol synchronization. The validation of combined chirped-LO and symbol synchronization can be another future research scope.
Chapter 6. Conclusions

2. **Optimize transceiver energy, accounting bandwidth-efficiency and demodulator trade-offs:** The transceiver system-circuit combined optimization for a duty-cycled radio can be further expanded to include the trade-off between bandwidth efficiency vs. demodulator SNR. Using the Shannon limit and a demodulator SNR vs. power consumption tradeoff, the transceiver minimum energy might be reduced further.

3. **Chirped-LO for localization:** The chirp clock usage for other functionalities in the WSNs system can be explored. For example, chirped clocks also have been proposed to help in sensor node localization. Although there are several localization schemes that are proposed for WSNs, accurate localization at low power is still a major challenge. The frequency difference between two synchronized chirp clock signals can indicate the travel time difference of those two signals from their respective transmitter when transmitters and the receiver are correctly synchronized. Distance can be derived from the frequency difference. This *chirped localization system* has a big similarity to the chirp-synchronization scheme proposed in this thesis. Therefore, the proposed chirped-LO system in this thesis has the potential to be added with the localization capability with a minimum amount of extra hardware. A more detailed analysis of its performance and low power implementation of the localization scheme is a possible future research problem.

4. **High robustness together with high data-rate:** In this thesis, the chirped-LO interference robustness is shown together with an ultra low power operation. However, at higher data rate, the interference robustness is reduced because of less bandwidth spread in a bit-period. Circuit design improvements to achieve interference robustness along with a higher data rate will be a very interesting target for future research. One possible way to improve performance at high data rate is to use a more accurate chirped clock, although this may cause extra power consumption. The accuracy of the chirped-LO generation can be improved by improving the linearity of the oscillator bias current vs. frequency characteristics and by improving the matching of the current DAC in the DCO.

5. **Effect of non-idealities in chirped-LO communication:** In this thesis a simplified analysis is done for the BER of the chirped-LO FSK and chirped-LO PSK systems. There is a scope for further analysis to understand the effect of oscillator nonlinearity and phase noise on the system performance. Analyzing the effect of those non-idealities on the chirped-LO communication can help to improve the performance of the proposed system further.
6. **Automated chirped-LO tuning targeting a more flexible system:** In this thesis the LO frequency is corrected to a predefined value in both receiver and transmitter. Therefore in this case a receiver can not receive a chirped-LO modulated (FSK or PSK) signal from a transmitter with a different start frequency and chirp frequency-time slope. A more flexible system can be achieved if the receiver LO can automatically scan the transmitter chirp clock characteristic and finds the starting frequency and chirp slope automatically. Although this will cost extra energy, the resulting system can find several other applications where more energy is available and interference close to the carrier frequency is a major concern.

7. **Use of more advanced CMOS technology to reduce energy further:** The receiver architecture and circuit topologies proposed here are expected to reduce receiver power consumption with the use of more advanced CMOS technology. The passive mixer power consumption should reduce similarly to the power reduction in a digital circuits due to CMOS scaling. The power consumption of a ring oscillator also reduces as the MOS capacitance reduces. The FSK demodulator, chirp generator and frequency correction loop are digital, so their power consumption is expected to reduce with the reduction of technology feature size. Therefore, most of the blocks in the designed receiver are expected to reduce power consumption at a more advanced CMOS technology.

8. **Analysis of the effects of multi-path fading and co-channel interferences in chirped-LO communication:** Other future extension of this work could be to investigate and analyze the effects of multi-path fading on the chirped LO system and compare with the multi-path fading effect on the non-chirped narrow-band communication. Also the effects of co-channel interferences are not analyzed in detail in this work. It would be very interesting to analyze and simulate these effects in detail especially for multi-channel chirped-LO communication systems.
Appendix A

Power consumption and Noise tradeoff in Receiver Frontend

A.1 Noise-power tradeoff in a Passive Mixer

For a passive mixer circuit, shown in Figure A.1, the noise factor can be written as [108]:

\[ F_M = F_{\text{min}} + \frac{R_{\text{ON}}}{R_S} \]  

(A.1)

where \( R_{\text{ON}} \) is the on resistance of the mixer switched used, \( F_{\text{min}} \) is the minimum noise factor and \( R_S \) is the source resistance. Assuming the device is in its linear region with drain to source voltage much smaller than the gate to source voltage, \( V_{GS} \), the ON resistance of a nMOS switch can be expressed as:

\[ R_{\text{ON}} = \frac{L}{\mu C_{\text{OX}} W (V_{GS} - V_{TH})} \]  

(A.2)

where \( W \) and \( L \) are the width and length of the mixer switch device respectively, \( C_{\text{OX}} \) is the MOS oxide capacitance in unit area and \( V_{TH} \) is the threshold voltage of a MOS transistor. Although the passive mixer does not consume static power itself, it capacitively loads the LO (or LO buffer) and contributes to the oscillator dynamic power consumption. The power
Appendix A. Power consumption and Noise tradeoff in Receiver Frontend

Figure A.1: Passive mixer (four phase) in a quadrature receiver

added to the oscillator or its buffer due to the passive mixer can be represented as:

\[ P_M = C_{MIX} V_S V_{DD} f_{osc} \]  \hspace{1cm} (A.3)

where \( V_S \) is the voltage swing (peak-to-peak) and \( f_{osc} \) is the frequency of the clock signal of the mixer, and \( C_{MIX} \) is the load capacitance of the mixer seen by the clock. Here, \( C_{MIX} \) assumes to be dominated by the gate capacitance and is equal to \( N_{mix} W L C_{OX} \), where \( N_{mix} \) is the number of mixer switches. Using this and (A.1), (A.2) and (A.3), the following relation can be obtained:

\[ P_M = \frac{L^2 V_S V_{DD} f_{osc}}{\mu (V_{GS} - V_{TH}) R_S} \frac{N_{mix}}{(F_M - F_{min})} \]  \hspace{1cm} (A.4)

From (A.4), the passive mixer power and noise factor can be related as \( P_M = \frac{K_M}{F_M - F_{min}} \), where \( K_M \) is constant for a given technology, supply voltage, topology and biasing. Noise factor is then: \( F_M = \frac{K_M}{P_M} + F_{min} \). For the circuits shown in Figure A.1, the simulated (65 nm CMOS process) and the modeled curve are shown in Figure A.2. There are two lines of the modeled
A.2 Power Optimization for two cascaded blocks

Figure A.2: Passive mixer power and noise factor tradeoff; Simulation result vs. modeled relation

noise figure corresponding to $F_{\text{min}} = 2.5$ and $F_{\text{min}} = 1$. The solid line shows the best fit to the simulation results with $K_M = 0.5 \text{ mW}$ and $F_{\text{min}} = 2.5$. The simplified case of $F_{\text{min}} = 1$ also shows a good fit with the simulation for the low power regions. Therefore (A.4) can be simplified with $F_{\text{min}} = 1$ for ultra low power designs.

For a three phase mixer, both the noise figure and power consumption is reduced. Therefore the value of $K_M$ should be comparable to the value of four phase mixer for a given technology.

### A.2 Power Optimization for two cascaded blocks

Consider two cascaded circuit blocks, as shown in Figure A.3, are to be optimized for power consumption for a given required noise factor. The noise factor of the two circuit blocks are modeled as:

$$F_L = 1 + \frac{K_L}{P_L}, \quad F_M = 1 + \frac{K_M}{P_M} \quad (A.5)$$

The overall receiver noise factor of these two blocks is given by the Friis equation [115]:

$$F_R = F_L + \frac{F_M - 1}{G_L} \quad (A.6)$$
where $G_L$ is the available power gain of the LNA. All the noise factors are expressed with respect to a source resistance of $R_S$. The target is to obtain the condition which minimizes the total power, $P_{LM} = P_L + P_M$ for a given overall noise factor $F_R$. This condition will dictate the optimum power (or noise factor) distribution in these two blocks. To derive the optimum condition, $P_{LM}$ is expressed in terms of $F_L$ using (A.5) and (A.6) as:

$$P_{LM} = \frac{K_L}{F_L - 1} + \frac{K_M}{F_M - 1}$$

$$= \frac{K_L}{F_L - 1} + \frac{K_M}{(F_R - F_L)G_L}$$

(A.7)

Differentiating (A.7) with respect to $F_L$ and equating it with zero, the $F_L$ for minimum power condition is obtained as:

$$F_{Lopt} = \frac{F_R \sqrt{K_L} G_L + \sqrt{K_M}}{\sqrt{K_L} G_L + \sqrt{K_M}}$$

(A.8)

and the power at that condition can be shown as:

$$P_{LMopt} = \frac{(\sqrt{K_L} G_L + \sqrt{K_M})^2}{G_L(F_R - 1)}$$

(A.9)

Therefore at the optimized power condition, the overall receiver power and noise factor can be related as:

$$P_{LM} = \frac{K_{RX}}{(F_R - 1)}$$

(A.10)
A.2. Power Optimization for two cascaded blocks

where $K_{RX}$ is a constant depending on the LNA, mixer noise-power constants and LNA gain. Concluding, we can say that the power consumption of a cascade of stages has the same dependence on targeted noise factor as a single stage, if optimal distribution of power between the stages is achieved.
Appendix B

A Synchronization Mechanism for Chirped Communication

The chirped carriers in the transmitter and receiver have to be time-synchronized for the proposed chirped-LO communication to work. In this appendix, a synchronization method for the chirped-LO communication is proposed.

To represent the unsynchronized clocks within the TX and RX, the chirp clock signal represented in (4.4) is modified for the TX and RX separately as:

\[ s_{tx}(t) = \sqrt{2P} \cos \left( 2\pi f_S t + \pi \beta t^2 + 2\pi \beta (-\theta_{tx}) t + \phi_t \right) \]  
\[ s_{rx}(t) = \sqrt{2} \cos \left( 2\pi f_S t + \pi \beta t^2 + 2\pi \beta (-\theta_{rx}) t + \phi_r \right) \]  

where the chirped signal phases (in time unit) are \( \theta_{tx} \) and \( \theta_{rx} \) for the TX and RX respectively, \( s_{tx} \) and \( s_{rx} \) are chirped signals as shown in Figure B.1, \( P \) is the (transmitted) signal power at the input of the receiver and the RX LO power is assumed to be unity. The aim of the synchronization is to align the RX chirp phase \( \theta_{rx} \), as close as possible to the TX chirp phase \( \theta_{tx} \). Both chirp signals are assumed to have the same frequency-time slope (or chirp-rate) \( \beta \) and the same starting frequency \( f_S \) as agreed and known before initiating the communication between the TX and RX. As the starting frequency is fixed, the TX and RX LO can achieve the starting frequency (frequency synchronization) by one-time calibration before starting the chirped communication. Without loss of generality, it can be assumed that \( \theta_{rx} = 0, \theta_{tx} = \Delta \theta \). The frequency difference of the TX and RX chirped-LO signal is a function of \( \Delta \theta \). Note that this frequency difference can be obtained by a
Appendix B. A Synchronization Mechanism for Chirped Communication

Figure B.1: Chirp synchronization circuit block diagram for the chirped-LO communication; circuit for RX mixer and low pass filter (LPF) combination, commonly used in receivers. Based on this observation, a synchronization scheme is proposed as shown in Figure B.1. During the synchronization process, the TX is assumed to transmit an unmodulated chirped carrier. The received TX chirp and the RX chirp are mixed and low pass filtered in the receiver. The signal after the LPF, \( q(t) \) can be related to the phase difference using (B.1) and (B.2)

\[
q(t) = \begin{cases} 
\sqrt{P} \cos(2\pi\beta(-\Delta\theta)t + \delta\phi) & \text{when } 0 < t < \Delta\theta \\
\sqrt{P} \cos(2\pi\beta(T_{CH} - \Delta\theta)t + \delta\phi) & \text{when } \Delta\theta < t < T_{CH}
\end{cases}
\]  

(B.3)

where \( \delta\phi = \phi_t - \phi_r \), \( \Delta\theta > 0 \) and the gain of the mixer and LPF is assumed to be one. The
two cases shown here can be visualized by the frequency vs. time plot of the TX and RX chirped clocks, as shown in Figure B.2. The difference frequency, sync-IF, is shown in the bottom. For $\Delta \theta > 0$, the frequency of the $q(t)$ signal can be rewritten as:

$$F_q(t) = \begin{cases} 
-\beta \Delta \theta, & \text{when } 0 < t < \Delta \theta \\
\beta (T_{CH} - \Delta \theta), & \text{when } \Delta \theta < t < T_{CH}
\end{cases}$$  

(B.4)

because $F_q(t)=0$ when $\Delta \theta=0$.

Similarly for $\Delta \theta < 0$, an equation of $q(t)$ can be obtained, which lead to:

$$F_q(t) = \begin{cases} 
\beta \Delta \theta, & \text{when } 0 < t < T_{CH} - \Delta \theta \\
-\beta (T_{CH} - \Delta \theta), & \text{when } T_{CH} - \Delta \theta > t > T_{CH}
\end{cases}$$  

(B.5)

Among the two possible sync-IF frequencies, in the example illustrated in Figure B.2, the lower frequency occupies more time in $T_{CH}$. This time duration is inversely proportional to the IF frequency. Hence, the integrated power also is inversely proportional to the frequency as shown in Figure B.3. In this figure the LPF effect is not considered. Therefore, there is always a frequency component between $[-B_{CH}/2$ to $B_{CH}/2]$, and this is the dominant one. Therefore the required LPF bandwidth is $B_{CH}/2$, i.e. half of the chirp bandwidth. When the phase difference, $\Delta \theta$ is close to $T_{CH}/2$, the output power of both frequencies are close to each other.

The frequency difference between the two chirped clock signals is extracted by a combination of an ADC and a Fast Fourier Transform (FFT) block (Figure B.1). The ADC converts the signal $q(t)$ from analog to digital. The FFT block outputs the frequency

![Figure B.3: Sync IF output power as a function of sync IF frequency assuming LPF cutoff high enough.](image-url)
Appendix B. A Synchronization Mechanism for Chirped Communication

information of the digitized signal. The output of the FFT block is converted to time delay by a digital-to-time converter in the control block. The chirp clock is generated by a analog or digital ramp signal at the input of a oscillator. A digitally controlled oscillator (DCO) is used here as shown in the figure. The time information from the control block changes the phase of the chirp by controlling the ramp signal.

To have a low power implementation, the frequency detection should be as fast as possible without operating too much hardware. Two possible options can be considered for a low power implementation of this scheme. Either by a real FFT block doing FFT operations twice in one chirp period to detect the magnitude and the sign of the frequency difference, $\beta\Delta\theta$, or a complex FFT block utilizing the I and Q path of the receiver, immediately differentiating between the positive and negative frequencies, and can extract the phase difference accordingly. For more details on the synchronization methods please refer to [97].
# Appendix C

## List of Abbreviations

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AC</td>
<td>Alternating Current</td>
</tr>
<tr>
<td>ADC</td>
<td>Analog to Digital Converter</td>
</tr>
<tr>
<td>AWGN</td>
<td>Additive White Gaussian Noise</td>
</tr>
<tr>
<td>BER</td>
<td>Bit Error Ratio</td>
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<tr>
<td>BFSK</td>
<td>Binary Frequency Shift Keying</td>
</tr>
<tr>
<td>BPSK</td>
<td>Binary Phase Shift Keying</td>
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<tr>
<td>CML</td>
<td>Current Model Logic</td>
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<tr>
<td>CMOS</td>
<td>Complementary Metal Oxide Semiconductor</td>
</tr>
<tr>
<td>COTS</td>
<td>Commercial Off-The-Shelf</td>
</tr>
<tr>
<td>CSS</td>
<td>Chirped Spread Spectrum</td>
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<tr>
<td>DAC</td>
<td>Digital to Analog Converter</td>
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<tr>
<td>DCO</td>
<td>Digital Controlled Oscillator</td>
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<tr>
<td>DFT</td>
<td>Discrete Fourier Transform</td>
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<tr>
<td>DR</td>
<td>Data Rate</td>
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<tr>
<td>DTGL</td>
<td>Dynamic Transmission Gate Logic</td>
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<tr>
<td>DSSS</td>
<td>Direct Sequence Spread Spectrum</td>
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<tr>
<td>FCL</td>
<td>Frequency Correction Loop</td>
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<tr>
<td>FFT</td>
<td>Fast Fourier Transform</td>
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<tr>
<td>FF</td>
<td>Flip-flop</td>
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<tr>
<td>FoM</td>
<td>Figure of Merit</td>
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<tr>
<td>FSK</td>
<td>Frequency Shift Keying</td>
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<tr>
<td>FHSS</td>
<td>Frequency Hopping Spread Spectrum</td>
</tr>
<tr>
<td>IC</td>
<td>Integrated Circuits</td>
</tr>
<tr>
<td>IEEE</td>
<td>Institute for Electrical and Electronic Engineers</td>
</tr>
<tr>
<td>IIP3</td>
<td>Third Order Input Intercept Point</td>
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<tr>
<td>IF</td>
<td>Intermediate Frequency</td>
</tr>
<tr>
<td>ISM</td>
<td>Industrial Scientific Medical</td>
</tr>
<tr>
<td>ISR</td>
<td>Interference to Signal Ratio</td>
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<tr>
<td>LNA</td>
<td>Low Noise Amplifier</td>
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<tr>
<td>LPF</td>
<td>Low Pass Filter</td>
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<tr>
<td>LO</td>
<td>Local Oscillator</td>
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<tr>
<td>OFDM</td>
<td>Orthogonal Frequency Division Multiplexing</td>
</tr>
<tr>
<td>OOK</td>
<td>On-Off Keying</td>
</tr>
<tr>
<td>MEMS</td>
<td>Micro Electro Mechanical System</td>
</tr>
<tr>
<td>MAC</td>
<td>Media Access Control</td>
</tr>
<tr>
<td>NF</td>
<td>Noise Figure</td>
</tr>
<tr>
<td>nMOS</td>
<td>n-type Metal Oxide Semiconductor</td>
</tr>
<tr>
<td>OOK</td>
<td>On-Off Keying</td>
</tr>
<tr>
<td>OSI</td>
<td>Open System Interconnection model</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed Circuit Board</td>
</tr>
<tr>
<td>pMOS</td>
<td>p-type Metal Oxide Semiconductor</td>
</tr>
<tr>
<td>PLL</td>
<td>Phase Lock Loop</td>
</tr>
<tr>
<td>PSK</td>
<td>Phase Shift Keying</td>
</tr>
<tr>
<td>PTAT</td>
<td>Proportional to Absolute Temperature</td>
</tr>
<tr>
<td>QLP</td>
<td>Quad Flat Package</td>
</tr>
<tr>
<td>QFN</td>
<td>Quad-flat No-leads</td>
</tr>
<tr>
<td>QPSK</td>
<td>Quadrature Phase Shift Keying</td>
</tr>
<tr>
<td>RC</td>
<td>Resistor-Capacitor</td>
</tr>
<tr>
<td>RADAR</td>
<td>RAdio Detection And Ranging</td>
</tr>
<tr>
<td>RAM</td>
<td>Random Access Memory</td>
</tr>
<tr>
<td>RF</td>
<td>Radio Frequency</td>
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<tr>
<td>RFID</td>
<td>Radio frequency Identification</td>
</tr>
<tr>
<td>ROM</td>
<td>Read Only Memory</td>
</tr>
<tr>
<td>RSSI</td>
<td>Received Signal Strength Indicator</td>
</tr>
<tr>
<td>RX</td>
<td>Receiver</td>
</tr>
<tr>
<td>SAW</td>
<td>Surface Acoustic Wave</td>
</tr>
<tr>
<td>SIR</td>
<td>Signal to Interference Ratio</td>
</tr>
<tr>
<td>SNIR</td>
<td>Signal to Noise and Interference Ratio</td>
</tr>
<tr>
<td>SNR</td>
<td>Signal to Noise Ratio</td>
</tr>
<tr>
<td>SoC</td>
<td>System on Chip</td>
</tr>
<tr>
<td>TBP</td>
<td>Time Bandwidth Product</td>
</tr>
<tr>
<td>TDMA</td>
<td>Time Division Multiple Access</td>
</tr>
<tr>
<td>TSPC</td>
<td>True Single Phase Clock</td>
</tr>
<tr>
<td>TRX</td>
<td>Transceiver</td>
</tr>
<tr>
<td>TX</td>
<td>Transmitter</td>
</tr>
<tr>
<td>ULE</td>
<td>Ultra Low Energy</td>
</tr>
<tr>
<td>ULP</td>
<td>Ultra Low power</td>
</tr>
<tr>
<td>USB</td>
<td>Universal Serial Bus</td>
</tr>
<tr>
<td>UWB</td>
<td>Ultra Wide Band</td>
</tr>
<tr>
<td>VCO</td>
<td>Voltage Controlled Oscillator</td>
</tr>
<tr>
<td>WLAN</td>
<td>Wireless Local Area Networks</td>
</tr>
<tr>
<td>WSN</td>
<td>Wireless Sensor Networks</td>
</tr>
<tr>
<td>WuRX</td>
<td>Wake-up Receiver</td>
</tr>
<tr>
<td>XTA/XOSC</td>
<td>Crystal Oscillator</td>
</tr>
</tbody>
</table>
## Appendix D

### List of Variables

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<tr>
<th>Variable</th>
<th>Description</th>
</tr>
</thead>
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<tr>
<td>( \alpha )</td>
<td>Signal to Interference power ratio (SIR)</td>
</tr>
<tr>
<td>( \alpha_{sw} )</td>
<td>Switching activity of a node capacitance</td>
</tr>
<tr>
<td>( \beta )</td>
<td>Chirped clock frequency vs. time slope ( \frac{df}{dt} ) or chirp-rate</td>
</tr>
<tr>
<td>( \eta )</td>
<td>TX power amplifier efficiency</td>
</tr>
<tr>
<td>( \Delta f )</td>
<td>Frequency difference between the BFSK tones</td>
</tr>
<tr>
<td>( \Delta \theta )</td>
<td>Time delay between the TX and RX chirped-LO signal</td>
</tr>
<tr>
<td>( \gamma_c )</td>
<td>Ratio of drain to gate capacitance of a MOS transistor</td>
</tr>
<tr>
<td>( \phi )</td>
<td>Initial phase of a sinusoidal signal, ( \phi_L ) and ( \phi_R ) for TX and RX LO respectively</td>
</tr>
<tr>
<td>( \phi_i )</td>
<td>Initial phase of an interferer</td>
</tr>
<tr>
<td>( \phi_{up} )</td>
<td>Phase of a up chirp signal</td>
</tr>
<tr>
<td>( \mu )</td>
<td>Electron mobility of a nMOS device</td>
</tr>
<tr>
<td>( \sigma_{\text{mix}} )</td>
<td>Timing jitter standard deviation due to device mismatch</td>
</tr>
<tr>
<td>( \sigma_{\text{DTG-FF}} )</td>
<td>Mismatch-jitter variance (variation in FF delay)</td>
</tr>
<tr>
<td>( \sigma_{\text{CML-FF}} )</td>
<td>Timing jitter standard deviation of CML flipflop due to device mismatch</td>
</tr>
<tr>
<td>( \sigma_{\text{DTG-FF}} )</td>
<td>Timing jitter standard deviation of DTG flipflop due to device mismatch</td>
</tr>
<tr>
<td>( \sigma_{\text{Vf}} )</td>
<td>Standard deviations ( Vf ) due to device mismatch</td>
</tr>
<tr>
<td>( \sigma_{\text{K} _n} )</td>
<td>Standard deviations ( K_n ) due to device mismatch</td>
</tr>
<tr>
<td>( \sigma_{\text{DTG-FF}}^2 )</td>
<td>Mismatch jitter of a DTG flipflop</td>
</tr>
<tr>
<td>( \sigma_{\text{CML}}^2 )</td>
<td>Mismatch jitter of a CML flipflop</td>
</tr>
<tr>
<td>( \theta )</td>
<td>Initial phase of the chirp repeat cycle; ( \theta_L ) and ( \theta_R ) for TX and RX respectively</td>
</tr>
<tr>
<td>( \omega_{up} )</td>
<td>Angular frequency of a up chirp signal</td>
</tr>
<tr>
<td>( \omega_{IF} )</td>
<td>Angular frequency in the IF stage of a receiver</td>
</tr>
<tr>
<td>( A )</td>
<td>Clock signal amplitude. ( A_0, A_1 20, A_2 40 ) are three phase clock signals.</td>
</tr>
<tr>
<td>( A_i )</td>
<td>Amplitude of the interference frequency components</td>
</tr>
<tr>
<td>( A_{VT} )</td>
<td>MOS threshold voltage mismatch parameter</td>
</tr>
<tr>
<td>( A_{\text{K}_n} )</td>
<td>( K_n ) mismatch constant</td>
</tr>
<tr>
<td>( A_R )</td>
<td>Resistor mismatch constant</td>
</tr>
<tr>
<td>( B )</td>
<td>Bandwidth of a signal</td>
</tr>
<tr>
<td>( BER )</td>
<td>Bit error ratio</td>
</tr>
</tbody>
</table>
Appendix D. List of Variables

<table>
<thead>
<tr>
<th>Variable</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$B_i$</td>
<td>Interference signal bandwidth</td>
</tr>
<tr>
<td>$B_{CH}$</td>
<td>Bandwidth of a chirped clock</td>
</tr>
<tr>
<td>$b_{CH}$</td>
<td>Bandwidth of a chirped clock in one bit period</td>
</tr>
<tr>
<td>$C_{gs}$</td>
<td>MOS gate capacitance</td>
</tr>
<tr>
<td>$C_{gn}$</td>
<td>nMOS gate capacitance</td>
</tr>
<tr>
<td>$C_{MIX}$</td>
<td>Mixer switch capacitance loading LO</td>
</tr>
<tr>
<td>$C_M$</td>
<td>Value of the capacitor used for input matching</td>
</tr>
<tr>
<td>$C_L$</td>
<td>Load capacitance</td>
</tr>
<tr>
<td>$C_{int}$</td>
<td>Internal capacitance arising at the load (of flipflop)</td>
</tr>
<tr>
<td>$C_{ox}$</td>
<td>MOS gate oxide capacitance per unit area</td>
</tr>
<tr>
<td>$c$</td>
<td>Speed of light in vacuum, $=2.99792458 \times 10^8$ m/s</td>
</tr>
<tr>
<td>$d$</td>
<td>Communication distance</td>
</tr>
<tr>
<td>$d_o$</td>
<td>Normalized overdrive ratio of $V_{OD}$ w.r.t. $V_{DD}$</td>
</tr>
<tr>
<td>$E_T$</td>
<td>Receiver energy consumption</td>
</tr>
<tr>
<td>$E_{T1}$</td>
<td>TRX energy consumption averaged per second/Average power consumption</td>
</tr>
<tr>
<td>$E_{min}$</td>
<td>Minimum energy of TRX. (minimum of $E_T$)</td>
</tr>
<tr>
<td>$E_b$</td>
<td>Energy per bit period</td>
</tr>
<tr>
<td>$e_{clk}$</td>
<td>Clock error as a fraction of clock period</td>
</tr>
<tr>
<td>$F_L$</td>
<td>Noise factor of LNA</td>
</tr>
<tr>
<td>$F_M$</td>
<td>Noise factor of Mixer</td>
</tr>
<tr>
<td>$F_R$</td>
<td>Noise factor of receiver front-end</td>
</tr>
<tr>
<td>$F_S$</td>
<td>Starting (Lower level) frequency of chirped-LO signal</td>
</tr>
<tr>
<td>$F_{SP}$</td>
<td>Sampling frequency</td>
</tr>
<tr>
<td>$F_E$</td>
<td>Ending (Higher level) frequency of chirped-LO signal</td>
</tr>
<tr>
<td>$F_{CML}$</td>
<td>CML topology function</td>
</tr>
<tr>
<td>$F_{DTG}$</td>
<td>DTG topology function</td>
</tr>
<tr>
<td>$F_{LO}$</td>
<td>Local Oscillator frequency (also $f_{LO}$)</td>
</tr>
<tr>
<td>$F_{RF}$</td>
<td>RF signal frequency</td>
</tr>
<tr>
<td>$F_W$</td>
<td>Noise factor of the wakeup radio</td>
</tr>
<tr>
<td>$f_o$</td>
<td>Output clock frequency</td>
</tr>
<tr>
<td>$f_R$</td>
<td>Starting (lower level) frequency of the received chirped clock</td>
</tr>
<tr>
<td>$f_T$</td>
<td>MOS unity gain frequency (default for nMOS)</td>
</tr>
<tr>
<td>$f_c$</td>
<td>Center frequency of chirped-LO signal (also $f_C$)</td>
</tr>
<tr>
<td>$f_{lo}$</td>
<td>Lowest frequency component of interference</td>
</tr>
<tr>
<td>$f_i$</td>
<td>Input frequency of a frequency divider (Chapter 3)</td>
</tr>
<tr>
<td>$f_i$</td>
<td>Frequency of an interferer (Chapter 5)</td>
</tr>
<tr>
<td>$F_{kernel}$</td>
<td>Noise factor of passive mixer kernel</td>
</tr>
<tr>
<td>$F_{min}$</td>
<td>Minimum noise factor</td>
</tr>
<tr>
<td>$F_{opt}$</td>
<td>Optimum noise factor for minimum energy</td>
</tr>
<tr>
<td>$f_{pf}$</td>
<td>Cutoff frequency of a low-pass-filter</td>
</tr>
<tr>
<td>$f_{osc}$</td>
<td>Oscillator frequency</td>
</tr>
<tr>
<td>$f_s$</td>
<td>Sampling frequency</td>
</tr>
<tr>
<td>$FoM_{CML,FF}$</td>
<td>Figure of merit (power*jitter) of CML flipflop</td>
</tr>
<tr>
<td>$FoM_{DTG,FF}$</td>
<td>Figure of merit of a per flipflop in a CML divider</td>
</tr>
<tr>
<td>$FoM_{CML,FF}$</td>
<td>Figure of merit of a per flipflop in a DTG divider</td>
</tr>
<tr>
<td>$FoM_{CML,MPCG}$</td>
<td>Figure of merit of MPCG or divider consists of CML flipflops</td>
</tr>
</tbody>
</table>
Figure of merit of MPCG or divider consists of DTG flipflops.

- \( G_L \): Available power gain of LNA
- \( G_V \): Voltage gain (of the input matching network)
- \( G_r \): RX Antenna gain
- \( G_t \): TX antenna gain
- \( g_m \): Transconductance of a MOS device
- \( H_n \): Transfer function of passive mixer for nth harmonic
- \( h \): Hop number for communication
- \( h_{opt} \): Optimum hop number for energy minimization
- \( I_0 \): Power spectral density of interference
- \( I_B \): Bias current of a CML buffer
- \( I_L \): Bias current of a CML latch
- \( i(t) \): Time domain interference signal
- \( K_n \): \( K_n = \mu_n C_{ox} W / L \)
- \( K_p \): \( K_p = \mu_p C_{ox} W / L \)
- \( K_D \): DCO frequency divided by input code
- \( K_I \): Noise-power constant of LNA; power consumed to achieve noise factor=2
- \( K_{FD} \): Receiver noise figure and datarate constant
- \( K_M \): Noise-power constant of mixer
- \( K_{BW} \): Bandwidth efficiency defined by datarate divided by bandwidth
- \( K_{RX} \): Noise-power constant of receiver frontend
- \( K_{M} \): Noise-power constant of mixer
- \( LB \): Link budget of the communication link
- \( L \): Length of a MOSFET device
- \( L_M \): Value of the inductor used for input matching
- \( M \): Number of phases required in a Multiphase clock generator or divider
- \( m(t) \): Message signal
- \( m \): Sub-threshold slope factor
- \( N \): Number of phases in the partial band interference
- \( N_s \): Total number of sampling points in time domain simulation
- \( N_b \): Number of bits per packet
- \( N_{mix} \): Number of passive mixer switches
- \( N_0 \): Power spectral density of (white) Gaussian noise
- \( N_W \): Number of bits required to transmit to wakeup the main radio
- \( NF \): Noise figure
- \( n \): Path-loss exponent (Chapter 2), number of phases (Chapter 5)
- \( n_b \): Number of bits in one chirp-time, \( T_{CH} \)
- \( P \): Signal power in Appendix-B
- \( P_d \): Power dissipation in general; power dissipation of flipflop for Chapter 3
- \( P_B \): Baseband power constant of the receiver
- \( P_{CML-FF} \): Power consumption of a CML flipflop
- \( P_{DTG-FF} \): Power consumption of a DTG flipflop
- \( P_{DTG-INBUF} \): Power consumption of a buffer used in DTG MPCG
- \( P_{CML-INBUF} \): Power consumption of a buffer used in CML MPCG
- \( P_I \): Interference power
- \( P_{INV} \): Power consumption of an inverter
Appendix D. List of Variables

$P_i(n)$ Interference power for $n$th bit in a chirped-LO
$P_F$ Total fixed power of TX and RX, independent of NF and datarate
$P_L$ Power consumption of the LNA in a receiver front end
$P_{LM}$ Power consumption of the LNA and mixer in a receiver front end
$P_M$ Power consumption of mixer
$P_{RF}$ Fixed RX power, independent of RX noise figure
$P_{RX}$ Receiver power consumption
$P_{OFF}$ Power consumption of TRX in sleep mode
$P_S$ Signal power (RX input)
$P_T$ Total transceiver power consumption
$P_{TF}$ Fixed TX power, independent of TX radiated power
$P_{TX}$ Transmitter power consumption
$P_{WB}$ Baseband power constant of the WuTRX
$P_{WBr}$ Baseband power constant of the WuRX
$P_{WBr}$ Baseband power constant of the TX communicating with WuRX
$Q(.)$ Q function
$Q$ Quality factor of a device or circuit
$q(t)$ Mixed and low-pass-filtered signal
$R$ Data rate of communication (TRX ON-mode)
$R_{DC}$ Rate of duty-cycling of the transceiver
$R_{opt}$ Optimum datarate for minimum energy consumption
$R_B$ Beacon rate
$R_{ON}$ ON resistance of a MOS device
$R_{in}$ Input resistance (of the receiver frontend)
$R_P$ Equivalent Parallel resistance of a LC circuit
$R_{PW}$ Wakeup radio packet rate
$R_S$ Source resistance
$R_{SW}$ Switch resistance (of a MOS device)
$R_W$ Datarate of the wakeup radio
$R_b$ Data/bit rate of TRX
$r_\mu$ pMOS-to-nMOS width ratio
$r_l$ Loading ratio, load capacitance by input capacitance
$r_M$ is the ratio of resistor and the input nMOS device area
$r_W$ Ratio between the interference bandwidth and chirp bandwidth ($B_i/B_{CH}$)
$S_{11}$ Input port voltage reflection coefficient
$SNR$ Signal to noise ratio
$SIR$ Signal to interference ratio
$SIR_{MIN}$ Minimum Signal to interference ratio required in the frequency range of interest
$s_{up}(t)$ Up signal time domain signal
$s_{down}(t)$ Down signal time domain signal
$s_{ud}(t)$ Up-down signal time domain signal
$T_{CH}$ Time duration of one chirp, say chirp-time
$t_s$ Receiver or transmitter startup time
$t_{CML}$ Clock to output delay of a CML flipflop
$t_{TG}$ Timing delay of a DTG flipflop
$t_{TG,AVG}$ Average of rise and fall Timing delay of a DTG flipflop
<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{SW}$</td>
<td>Wakeup radio startup time</td>
</tr>
<tr>
<td>$V_{DD}$</td>
<td>Power supply voltage</td>
</tr>
<tr>
<td>$V_{GS}$</td>
<td>Gate to source voltage of a MOS device</td>
</tr>
<tr>
<td>$V_{OD}$</td>
<td>Overdrive voltage of a MOS device</td>
</tr>
<tr>
<td>$V_S$</td>
<td>Voltage swing of a clock signal</td>
</tr>
<tr>
<td>$V_{TP}$</td>
<td>Threshold voltage of a pMOS device</td>
</tr>
<tr>
<td>$V_{TN}$</td>
<td>Threshold voltage of a nMOS device</td>
</tr>
<tr>
<td>$V_{TH}$</td>
<td>Threshold voltage of MOS device</td>
</tr>
<tr>
<td>$W$</td>
<td>Width of a MOS device</td>
</tr>
<tr>
<td>$W_B$</td>
<td>Width of the input transistors of a CML buffer</td>
</tr>
<tr>
<td>$W_L$</td>
<td>Width of the input transistors of a CML latch</td>
</tr>
<tr>
<td>$Z_{in}$</td>
<td>Input impedance of the receiver</td>
</tr>
</tbody>
</table>
Bibliography


[18] Sun Spot. URL "http://www.sunspotworld.com/".


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This thesis could not be possible without the help, support and contributions from many people. I would like to take this opportunity to thank them.

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Ramen Dutta
March, 2016
List of Publications


About the Author

Ramen Dutta received B.E. degree in Electronics and Telecommunication from Bengal Engineering College (IIEST), Shibpur, India in 2002. From 2002 to 2006 he worked at Alliance Semiconductor in Bangalore, India on mixed signal circuits for Static Random Access Memory (SRAM) ICs. He received MS (by research) degree from Indian Institute of Technology, Kharagpur in 2009 for his work on multiphase clock generation circuits. From July 2008 to February 2009 he worked at Kawasaki Microelectronics on Digital to Analog converters. From March 2009 to December 2013 he worked towards the Ph.D. degree on the subject of ultra low power and interference robust transceiver design for wireless sensor networks at the University of Twente, the Netherlands. From January 2014 he is working at Marvell Technologies in Switzerland on ADPLL and other clock generation circuits for wireless applications. His research interests include clock generation circuits, low power RF front-end circuits, wireless communication systems, and CMOS mixed signal circuits.

This thesis is the result of his Ph.D. research, conducted at the Integrated Circuit Design (ICD), Computer Architecture and Embedded Systems (CAES) and Telecommunication Engineering (TE) group under the CTIT Research Institute of the University of Twente.