Cancellation of OpAmp Virtual Ground Imperfections by a Negative Conductance applied to improve RF Receiver Linearity

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Abstract — High linearity CMOS radio receivers often exploit linear V-I conversion at RF, followed by passive down-mixing and an OpAmp-based Transimpedance Amplifier at baseband. Due to nonlinearity and finite gain in the OpAmp, virtual ground is imperfect, inducing distortion currents. This paper proposes a negative conductance concept to cancel such distortion currents. Through a simple intuitive analysis, the basic operation of the technique is explained. By mathematical analysis the optimum negative conductance value is derived and related to feedback theory. In- and out-of-band linearity, stability and Noise Figure are also analyzed. The technique is applied to linearize an RF receiver, and a prototype is implemented in 65 nm technology. Measurement results show an increase of in-band IIP3 from 9dBm to >20dBm, and IIP2 from 51 to 61dBm, at the cost of increasing the noise figure from 6 to 7.5dB and <10% power penalty. In 1MHz bandwidth, a Spurious-Free Dynamic Range of 85dB is achieved at <27mA up to 2GHz for 1.2V supply voltage.

Index Terms — Receiver linearity, interference robustness, compression, blocking, in-band and out-band IIP3, IIP2, mixer-first receiver architecture, transimpedance amplifier (TIA), negative conductance technique, CMOS, wideband base station receiver, software radio, software defined radio, cognitive radio.
I. INTRODUCTION

Linearity requirements on radio receivers become increasingly challenging, as the radio spectrum becomes more crowded. Moreover, there is a trend towards more wideband and more flexible radio hardware with less dedicated RF filtering (“Software Defined Radio”). As an example, Figure 1 plots IIP
requirements calculated for E-UTRA for a wideband base station receiver in three scenarios: wide area, local area and home [1]. Apart from the high 100MHz bandwidth, note the sudden step in IIP
requirements at the band-edge. Also note that less coverage area (home versus wide area), corresponds to higher in-band IIP but a smaller step to out-of-band IIP (i.e. around 16dB for home area versus 40dB for wide area). As a consequence of the lack of a reasonable transition band, on-chip analog filtering is ineffective to relax the IIP requirement, and off-chip filters are expensive. Depending on the blocker scenario, compression point requirements may or may not be affected. In this paper, we propose a circuit technique that can increase IIP simultaneously for in- and out-of-band, at roughly constant compression point. Receivers with high IIP are also very important for opportunistic dynamic spectrum access via a cognitive radio, as is exemplified in Figure 2 for a Digital TV band. Strong interferers (incumbent TV signals) may be present in directly adjacent channels, again making on-chip RF filtering ineffective. Again, high linearity is required also to prevent cross-modulation effects [2] from desensitizing the receiver. A part from the RF receivers, the spectrum sensing front-end also requires high in-band IIP in order to minimize the errors in detecting the empty channels in the spectrum.

Strong RF interference can easily clip baseband amplifiers, while higher required bandwidths limit the amount of available loop-gain for negative feedback. When pushing linearity, avoiding voltage gain at RF (See Figure 3) is instrumental [[3]-[8]]. Exploiting RF V-I conversion followed by passive down-mixing and then simultaneous I-V conversion and filtering at IF/baseband with OpAmps, an out-of-band IIP of up to +18dBm has been shown [[3],[4]]. Passive mixer-first architectures can even achieve up to +25dBm out-of-band IIP [7]. However in-band IIP is much worse, certainly at high gain. The best in-band IIP results that we found for receivers were +3.5dBm for [3] at 34dB gain and +11dBm for [6] at
19dB gain. Analysis shows that finite OpAmp gain can be a bottleneck, as a non-zero virtual ground node voltage can result in distortion currents. In [9], we recently proposed to exploit a negative conductance technique to cancel distortion currents. In this way, the design of the OpAmp is relaxed and its performance no longer needs to be a bottleneck. The use of a negative conductance has been proposed in [10] to realize TIA flicker noise shaping. Paper [10] also briefly mentions linearity improvement, but linearity benefits were not the focus there. In this paper we will analyze the benefits of a negative conductance, compare analysis to measurements and report some extra experimental results in addition to [9]. Section II presents an intuitive model to understand the basic distortion cancellation concept. Additionally, the optimum negative conductance value is derived by mathematical analysis and related to negative feedback theory. Section III analyses stability issues related to this negative conductance technique. A receiver design, in which the concept is exploited, is discussed in Section IV. The receiver noise figure analysis including the negative conductance contribution is discussed in section V. The analysis is verified by measurements in section VI, while results are also benchmarked to other high linearity receivers. Finally, section VII presents conclusions.

II. LINEARIZATION CONCEPT

To understand the OpAmp linearity limitation and the distortion cancellation technique intuitively, it is instructive to follow a 4-step approach to analyze what happens at the virtual ground node “VGND”, as illustrated in Figure 4 to Figure 8:

Step 1: Assume the RF V-I conversion and mixing are perfectly ideal (i.e. linear and infinite current source resistance for GM), we can use the equivalent baseband model in Figure 4 (omitting the downconversion for simplicity). Assuming a 2-tone input signal $V_S(f)$, the injected current $I_S(f)$ to the VGND node is linear, so without IM3 tones. Now, if the OpAmp handles large signals at a high but finite gain, its output stage will produce IM3 products at the OUT node, i.e. $V_{OUT}(f)$. However, as $I_S(f)$ has no IM3 and the feedback resistor $R_f$ is linear, the voltage over $R_f$ does not contain IM3 (assuming negligible
OPAMP input current). Consequently, the IM3 products of \( V_{VGND}(f) \) are in absolute sense equal to those of \( V_{OUT}(f) \) both in magnitude and phase. Let’s denote this “IM3 copy” effect in Figure 4 as “problem A”. Note that the two main tones of \( V_{VGND}(f) \) are much smaller than that of \( V_{OUT}(f) \), as the ratio \( V_{OUT}(f)/V_{VGND}(f) \) for linear terms is equal to the loop gain. As a consequence the ratio between the linear terms and the IM3 products at VGND node is much worse than at the OUT node, causing a more serious problem discussed next.

Step 2: Assume we add a finite output resistance \( R_O \) as shown in Figure 5. The nonlinear voltage \( V_{VGND}(f) \) over \( R_O \) now generates a nonlinear current \( I_O(f) \), and hence \( I_F(f) \) becomes nonlinear. This current is absorbed by the OpAmp output stage and increases IM3 at both \( V_{OUT}(f) \) and \( V_{VGND}(f) \). We will denote this “RO loading” effect on the VGND node in Figure 5 as “problem B”.

Step 3: Once one realizes the main cause for distortion current is \( V_{VGND}(f)/R_O \), it is easy to verify that adding a negative conductance with value \( G_O=1/R_O \) between VGND and ground can be a solution (see Figure 6). The negative conductance senses \( V_{VGND} \) and generates a copy of the distorted current \( I_O(f) \), which now flows in a “local circle” via the ground. Consequently, the current injected to the VGND node becomes linear again and we are back at the circuit of problem A, having solved problem B.

Step 4: Still, the OpAmp output voltage contains some IM3, equal to that on the VGND node. By slight overcompensation this IM3 contribution can also be cancelled. To show this, it is useful to model the floating resistor \( R_F \) with an equivalent network consisting of four single-ended linear transconductor blocks \( G_F \) (\( G_F=1/R_F \)), all referred to ground as shown in Figure 7 (a). The two shorted \( G_F \) blocks, indicated with a dashed ellipse, can be replaced by a simple \( R_F \) resistor to the ground (see Figure 7 (b)). Thus Figure 7 (c) results with \( R_{F-VGND} \) and \( R_{F-OUT} \), (loading resistances at the VGND node and the OUT node, respectively), \( G_{F-VGND} \) (the transconductance sensing \( V_{OUT} \) and injecting current to the VGND node), and \( G_{F-OUT} \) (the transconductance sensing \( V_{VGND} \) and injecting current to the OUT node). We assigned different names to \( G_F \) and \( R_F \) blocks in order to distinguish between their effects on nonlinearity.
at the VGND node and the OUT node separately. Figure 7 (c) clearly shows the loading effect of $R_F$ (i.e. $R_{F-VGND}$) at the VGND node. Now, when the negative conductance cancels this loading effect (see Figure 8), the injecting current of $G_{F-VGND}$ becomes equal to the linear current $I_S$. As $V_{OUT}=I_S/G_{F-VGND}=-I_S.R_F$, the OpAmp output voltage $V_{OUT}$ becomes linear. This way problem A is solved as well.

Overall, combining the solutions for problem A and B, the optimal total negative conductance is: $G_{TOTAL}=1/R_O+1/R_F$. To mathematically prove this optimum cancellation condition, the OpAmp (see Figure 9) is modeled as an OTA with nonlinear transconductance and also a nonlinear output resistance because we aim for high output swing:

\[ I_F = g_{m1}V_{IN} + g_{m3}V_{IN}^3 + g_{o1}V_O + g_{o3}V_O^3 \]  \hspace{1cm} (1)

In the model, we assume that the third order nonlinearities are more pronounced than the second order nonlinear terms, which is reasonable considering the OpAmp will be implemented in fully differential form. In the Appendix A, the nonlinear relation between $V_{OUT}$ and signal current $I_S$ is derived using the model in Figure 9. It can be expressed in terms of a linear ($\Omega_1$) and third-order nonlinear ($\Omega_3$) coefficient:

\[ V_{OUT} = \Omega_1 I_S + \Omega_3 I_S^3 \]  \hspace{1cm} (2)

The linear coefficient $\Omega_1$ is the I/V conversion gain:

\[ \Omega_1 = \frac{1}{\frac{1}{a} \left( \frac{1}{R_O} + \frac{1}{R_{F-VGND}} \right) + G_{F-VGND}} \]  \hspace{1cm} (3)

Where $(a)$ is a function of the linear terms of the OpAmp model (i.e. $g_{m1}$, $g_{o1}$) and the $R_F$ effects at the OUT node (i.e. $R_{F-OUT}$ and $G_{F-OUT}$). For very high $g_{m1}$, $(a)$ reaches $-\infty$. Consequently, the I/V conversion gain of (3) becomes $1/G_{F-VGND} = -R_F$.  

The third-order distortion coefficient ($\Omega_3$) is:

$$\Omega_3 = \frac{NL_3 \left(\frac{1}{R_O} + \frac{1}{R_{F-VGND}}\right)}{\left[\frac{1}{a \left(\frac{1}{R_O} + \frac{1}{R_{F-VGND}}\right) + G_{F-VGND}}\right]^4}$$

(4)

where ($NL_3$: see Appendix A) is related to the nonlinear terms of the OpAmp model and is a function of (i.e. $gm_1$, $gm_3$, $go_1$ and $go_3$) and the effect of $R_F$ on the OUT node (i.e. $R_{F-OUT}$ and $G_{F-OUT}$). Now, if the negative conductance technique cancels $1/R_O+1/R_{F-VGND}$ from (3) and (4) we see that $\Omega_1$ reaches $1/G_{F-VGND}=-R_F$ and $\Omega_3$ becomes zero (distortion is cancelled). Note that since the voltage swing at the VGND node is small, the effect of negative conductance nonlinearity can be very small.

The linearity benefit can also be verified by applying feedback theory to Figure 9 as shown in Figure 10, excluding GM. The feedback topology of the circuit is Voltage-Current Feedback [11]. The output voltage (i.e. $V_{OUT}$) is sensed and converted to a proportional feedback current $\beta V_{OUT}$, where $\beta=G_{F-VGND}$ (in Siemens). This feedback current is subtracted from the input current $I_S$ resulting in an error current $I_{error}=I_S-\beta V_{OUT}$ to be amplified by the block $A$. Here, $A=V_{OUT}/I_{error}$, where $A$ has the dimension of a transimpedance [$\Omega$]. It consists of all the blocks of Figure 9, excluding GM and $G_{F-VGND}$. Actually for finite $A$, there will be a non-zero $I_{error}$ due to the loading effect of $R_O$ and $R_{F-VGND}$ on the VGND node. Now the negative conductance increases the input impedance of the $A$ block to infinity by cancelling $R_O$ and $R_{F-VGND}$, so that $I_{error}$ becomes zero and $A=V_{OUT}/I_{error}=\infty$. Consequently, loopgain $A\beta$ goes to infinity and $V_{OUT}/I_S$ achieves its ideal value $1/\beta=R_F$, i.e. perfect linearity. We conclude that the negative conductance technique increases the loop gain by increasing the value of $A$. Also note that only a finite value for $G_o$ is needed to make the loopgain theoretically approach infinity, which is not possible by increasing $gm_1$ in the gain block. Although the feedback theory puts the application of a negative conductance technique in the right context, however the problem with control theory is that it assumes blocks with unilateral operation, which are sometimes not easy to identify (e.g. see Figure 10: feedback
resistor $R_F$ which is supposed to realize the $\beta$ block also becomes part of the A block). In compare to the feedback analysis, our analysis explains in a simple way how $IM_3$ is affected by $R_O$ and $R_F$.

To verify the OpAmp model, we fitted the model derived above to simulations done for the OpAmp that will be introduced later in this paper. Figure 11 shows a close agreement.

Now, before we proceed with detailed circuits design, we will first deal with a potential caveat of negative conductance: the risk of instability.

III. STABILITY ANALYSIS

We will consider two stability aspects: 1) the risk of oscillation, based on a small signal model, and 2) the risk of latch-up. Let us first look at the small signal behavior, referring to Figure 12. As the low-pass filtering is desired, $C_F$ is added as feedback capacitor. Capacitor $C_T$ models the total input capacitance to ground of the OpAmp $C_{IN-OpAmp}$ and other capacitance $C_O$ at the VGND node (see Figure 3). For simplicity, the OTA is modeled as a frequency dependent transconductance with a dominant pole at $\omega_O$ and infinite output impedance:

$$gm(s) = \frac{gm_o}{1 + \frac{s}{\omega_o}}$$  \hspace{1cm} (5)

Assuming no further loading at the OUT node, looking into the VGND node (see Figure 12), the impedance ($Z_{IN}$) consists of the reactance of $C_T$ in parallel to $1/gm(s)$:

$$Z_{IN} = \frac{1}{s C_T} // \frac{1}{gm(s)} = \frac{1}{s C_T} // \left[ \frac{1}{gm_o} + \frac{s}{gm_o \omega_o} \right]$$  \hspace{1cm} (6)

Therefore, a parallel RLC tank is seen looking into the VGND node. If the negative conductance would both cancel $1/R_O$ and $gm_o$, then oscillation would happen at a resonance frequency that depends on the
value of $C_T$ and L (i.e. $f_{res} = 1/(2\pi \sqrt{C_T L})$). However, note that the typical virtual ground impedance $1/gm_O$ will normally be much lower than $R_O$ and $R_F$. Thus, as the negative conductance $G_{Total}$ is designed to cancel $1/R_O$ and $1/R_F$, the point of small signal instability can be designed to be safely far away.

Let’s now look at the potential of latch-up of the OpAmp for a case that the negative conductance is too strong, i.e. it produces more current than needed after compensating the current in $R_O$. As shown in Figure 13, the negative conductance injects current via $R_F$ (i.e. $V_{VGND}G_{Latch-up-Risk}$) that needs to be handled by the OpAmp output stage in addition to the main current coming from $G_M$ (i.e. $I_S$):

$$I_{OpAmp-Latch-up-Risk} = I_S + V_{VGND} G_{Latch-up-Risk}$$

$$= I_S + \left[ \frac{1}{R_F-V_{VGND}} - G_{Latch-up-Risk} \right] + a G_{F-VGND}$$

\[ (7) \]

Where the relation between $V_{VGND}$ and $I_S$ is derived in Appendix B. Referring to Figure 13 and substituting $G_{Latch-up-Risk} = (1/R_F) + \Delta G$, in (7) gives the following relation:

$$I_{OpAmp-Latch-up-Risk} = I_S \left[ 1 - \frac{\Delta G + \frac{1}{R_F}}{\Delta G + \frac{a}{R_F}} \right]$$

\[ (8) \]

The OpAmp output stage current flows through $R_F$ and make a voltage drop. The peak of this voltage drop is around $VDD/2-V_{OpAmpOutputStage-OV}$, where $V_{OpAmpOutputStage-OV}$ is the over drive voltages of the OpAmp output stage transistors. Hence, if very strong negative conductance has been used (i.e. high $\Delta G$ in (8)), then the current of (8) becomes higher than the OpAmp output stage current capability and the latch-up occur.
IV. RECEIVER DESIGN

We will now apply the negative conductance idea to a high linearity zero-IF radio receiver architecture of Figure 3. To demonstrate the linearity potential of this technique, we will replace the active V-I conversion by a more linear fully passive mixer with resistors in series [4], as shown in Figure 14. Figure 15 shows the complete front-end IC schematic including the negative conductance. Using the equivalent model in Figure 5, we can model the RF part of each branch in I and Q as a grounded resistor $R_O$ and a transconductor $G_M$ referred to ground as denoted in Figure 15. However, as resistor $R_{RF}$ is in series with the mixer on-resistance $R_{ON-MIXER}$ and the virtual ground impedance $R_{VGND}$ of the OpAmp, the equivalent $G_M$ now equals $1/(R_{RF}+R_{ON-MIXER}+R_{VGND})$. This is chosen to be 20mS to realize RF input impedance matching of 50Ω, assuming perfect non-overlapping 25% duty-cycle clocks, so the RF-input continuously sees a conduction path to ground. The equivalent output impedance of the mixer at baseband now is $R_O=2(R_{BalUn}+R_{RF}+R_{ON-MIXER})$, where the factor 2 is due to the quadrature mixer with 25% duty cycle, connecting each I and Q baseband part to RF two times per LO cycle. To understand this point, let’s derive $R_O$ from the power that is delivered by a test voltage source (i.e. $V_{test}=V_a \cos(\omega_{LO}t)$) “looking back” in $R_O$ as shown in Figure 16. This source is connected to the first branch of the I-path. The current $I_{test}$ will flow through $R_{ON-MIXER}+R_{RF}+R_{BalUn}$ two times LO-cycle, hence we get:

$$P = \frac{1}{T_{LO}} \left[ \int_0^{T_{LO}} V_{test} I_{test} \, dt + \int_{T_{LO}}^{2T_{LO}} V_{test} I_{test} \, dt \right] = \frac{V_a^2}{4 (R_{ON-MIXER} + R_{BalUn} + R_{RF})}$$

This power must be equal to the power dissipation in $R_O$:

$$P = \frac{1}{T_{LO}} \int_0^{T_{LO}} \frac{V_{test}^2}{R_O} \, dt = \frac{V_a^2}{2R_O}$$

By equating (9) and (10), the following $R_O$ is derived:
In the derivation of $R_O$, the power is only balanced with the fundamental, while the effect of the 3rd and higher harmonics are neglected due to the existence of $C_O$ (see Figure 15).

Now, the 50Ω input impedance matching is implemented as a combination of series resistances $R_{RF}\approx12\Omega$, the up-converted impedances of the passive mixer switches $R_{ON-MIXER}\approx28\Omega$ plus the VGND impedance $R_{VGND}\approx7\Omega$. The passive mixer consists of simple NMOS switches. $C_O=8pF$ effectively shorts the LO leakage and high IF frequency components to ground. The TIA consists of a class-A input stage and a class-AB output stage, to maximize output swing (see Figure 17, [12] and [3]). Common mode feedback ensures biasing at VDD/2. The feedback impedance is $R_f=1.5k\Omega$ and $C_f=8pF$, to obtain 26dB voltage gain and a -3dB-bandwidth of 12MHz. The differential topology allows for a simple differential implementation of the negative conductance (right part of Figure 15) and high IIP2. To be able to measure what is the effect of different negative conductance values, -$G_O$ is implemented as a parallel array of identical “unit-transconductors”, digitally controllable via multiplier M, with transconductance steps of 0.2mS. Thus $M=28$ renders $G_O=5.6mS$ to compensate the nominal value of $R_O=180\Omega$ ($R_O=2(R_{BalUn}+R_{RF}+R_{ON-MIXER})=2(50+12+28)=180\Omega$).

We will now consider the noise degradation resulting from the introduction of the negative conductance. Actually this noise can be cancelled by a noise cancellation path [[13],[4]], however this is expected to result in a linearity bottleneck in the auxiliary noise cancellation path. Hence we will analyze the noise figure degradation and aim for minimizing the noise penalty.

V. Noise Figure Analysis (NF)

Receiver topologies with a passive mixer and transimpedance amplifier (TIA), can suffer from amplification of OpAmp noise [14]. The output referred OpAmp noise contribution can be written as:

$$R_O = 2(R_{ON-MIXER} + R_{BalUn} + R_{RF})$$

(11)
\[ V_{n-\text{OUT}}^2 = \left( 1 + \frac{R_F}{R_O} \right)^2 V_{n-\text{OpAmp}}^2 \]  

(12)

Where \( V_{n-\text{OpAmp}} \) refers to the (equivalent) input noise voltages of the OpAmp, \( R_O \) and \( R_F \) are as used in Figure 5. For our design \( R_F=1.5k\Omega \) and \( R_O=180\Omega \), then the amplification factor is equal to \((1+R_F/R_O)^2=87\). Often a high RF V/I conversion (GM-value) is used to achieve an overall noise figure around or below 3dB. Here we will use 20mS, the value desired for input impedance matching. Figure 18 shows a baseband model of Figure 14 with noise sources added. The noise of GM is represented by the current noise source (\( I_{n-Ro} \)) of \( R_O \). The noise of \( R_F \) is modeled via voltage noise source \( V_{n-RF} \), while \( I_{n-GTotal} \) represents the current noise source of the negative conductance. For simplicity, the OpAmp is modeled as a simple Transconductance (gm). To analyze the noise contributions of \( I_{n-Ro} \) and \( I_{n-GTotal} \) to the output voltage, \( \Omega_1 \) (i.e. the I/V conversion of the TIA (3)) is useful. The straightforward NF analysis shows:

\[ \text{NF} = 1 + \frac{1}{\left( \frac{1}{2} \Omega_1 \, \text{GM} \right)^2 R_S} \left[ \frac{1}{R_O} \left( 1 + \gamma G_{\text{Total}} \right) + \frac{V_{n-\text{OpAmp}}^2}{I_{n-RF}^2 R_O} \left( 1 + \frac{R_F}{R_O} \left( \frac{1}{R_O} - G_{\text{Total}} \right) \right)^2 + R_F \left( \frac{1}{\text{gm} \, R_F} - 1 \right)^2 \right] \]  

(13)

The first term between the square brackets in (13) shows that the negative conductance \( G_{\text{Total}} \) has a direct noise contribution to the output. Its noise contribution is scaled by \( \gamma \left( \frac{1}{2} \text{GM} \right)^2 R_S \). The “noise excess factor” \( \gamma \) can be minimized to around 2/3 (i.e. theoretically) by choosing a non-minimum channel length for the negative conductance transistors. Long-channel transistors are preferred for 1/f noise. We used 1\( \mu \)m channel length in this design. The second term is the mentioned amplification factor (12) of OpAmp noise including the negative conductance effect (\( G_{\text{Total}} \)). It is interesting to observe that this term reaches zero when the negative conductance reaches \( G_{\text{Total}} \). However, the direct noise contribution of the negative conductance is much higher than the canceled OpAmp noise contribution, hence the total noise figure of the circuit increases. We verified (13) by noise simulations using the OpAmp circuit of Figure 17. The NF is increased from 6 to 7.5 dB given that GM is equal to 20mS. Note that it is also possible to apply the
negative conductance in combination with an LNTA with higher GM and hence lower NF. In that case, the negative conductance can be lower, as $R_O > 1/GM$. However, then $IIP_3$ of the LNTA becomes a bottleneck.

VI. MEASUREMENT RESULTS AND BENCHMARKING

Figure 19 shows a photo of the implemented 65nm IC. The active area is $< 0.2 \text{ mm}^2$ including the clock circuit. Thick metal was used for $R_{RF}$ for high linearity and low spread.

The front-end achieves 26 dB gain (BalUn losses are de-embedded) at 1 GHz LO, over 24MHz bandwidth (BW), 12MHz on either side of LO. To demonstrate distortion cancelling, Figure 20 (a) shows the measured in-band $IIP_3$ at 150kHz tone spacing ($f_1=1004.1\text{MHz}$ and $f_2=1004.25\text{MHz}$) vs. M. $IIP_3$ clearly improves from around +9 dBm to +21 dBm!

The optimum $IIP_3$ of +21 dBm is located at $M = 32$, which fits to our theory $G_{Total}=1/R_O+1/R_F=1/1500+1/180=6.22\text{mS}$ so $M=6.22\text{mS}/0.2\text{mS}=31$ very well. Figure 20 (b) shows the IM3 curves versus power for three cases: $M=0$ (off), $M=28$ (cancelling of $I_O$, Figure 6) and $M=32$ (overall optimum $IIP_3$). Up to -22dBm input power (note: this power is high for an in-band signal), IM3 improves. The rise of distortion for high input powers $> -23$ dBm is due to the clipping of the OpAmp output stage to its 1.2V supply. The negative conductance was pushed to instability (i.e. latch-up of OpAmp output stage). This occurs at $M=45$ (see (8) $\Delta G=\Delta M x 0.2\text{mS}$), safely away from the optimum point by $\Delta M=45-32=13$. This shows a close agreement with our explanation in section III and with the simulations in Figure 21, which is done for the circuit of Figure 13. One tone input signal with power of -16 dBm is used. Around this input power, the OpAmp output stage begins to clip. According to our simulation, the latch-up occurs for $\Delta M \geq 14$. The same mechanism, discussed in section II, of this technique also improves $IIP_2$ by more than 10 dB as shown in Figure 22. Table I compares/summarizes the $IIP_2$ and $IIP_3$ improvement for three $M$ settings 0, 28 and 32. Note that the optimum linearity point will vary somewhat with Process, Voltage and Temperature (i.e. PVT). The analysis in this paper gives the relation between
the required negative conductance and the resistance values \( R_O \) and \( R_F \), which can be a basis for designing an automatic PVT correction circuit.

Figure 23 provides \( \text{IIP}_3 \) curves versus the frequency offset \( \Delta f \), with fixed 3.95MHz in-band \( \text{IM}_3 \) position. The negative conductance clearly increases the \( \text{IIP}_3 \) both in- and out-of-band (all-Band) with a worst case \( \text{IIP}_3 > +10 \) dBm. The reason behind less linearity improvement in the transition band can be understood considering the equivalent circuit earlier derived for stability analysis in Figure 12. The negative conductance cancels only the loading of \( R_O \) and \( R_F \). However, \( \text{gm}(s) \), \( C_F \) and \( C_T \) introduce frequency dependences. Consequently, the “loading effect” on the \( \text{VGND} \) node (see Figure 5) becomes frequency dependent and will introduce a phase shift compared with the (frequency independent) current generated by the negative conductance. This results in imperfect cancellation, i.e. less linearity improvement at high frequencies. This may be improved in the future by designing the negative conductance to be frequency dependent as well. Up to 10MHz, in-band \( \text{IIP}_3 \) is \( > +20 \) dBm, i.e. \( > 10 \) dB improvement thanks to the negative conductance. Then the \( \text{IIP}_3 \) declines from 12MHz to 135MHz, on the one hand because the OTA gain and hence its linearity degrades, but on the other hand also because the benefit from cancellation drops (the top line in Figure 23 drops faster, versus \( \Delta f \), than the bottom line). Note that the out-of-band \( \text{IIP}_3 \) at \( \Delta f > 450 \) MHz is again high, \(+ 18 \) dBm. This is because at high \( \Delta f \) (i.e. spacing between the carriers) the carriers are filtered due to the low pass filtering by \( C_F \), \( R_F \) and \( C_O \), hence less \( \text{IM}_3 \) products. In this region the negative conductance doesn’t result in any benefit anymore.

The compression point (CP) is around -13 dBm (hardly affected by \( M \) as shown in Figure 24). Due to the virtual ground, \( S_{11} \) is hardly affected by the negative conductance and Figure 25 (a) shows that \( S_{11} < -25 \) dB. Noise is more worrisome, but depending on the application some degradation may be acceptable, provided that the overall SFDR still improves (i.e. \( \text{IIP}_3 \) in dBm should improve more than \( \text{NF} \) in dB degrades). Figure 25 (b) shows that \( \text{NF} \) increases from 6.2 dB at \( M=0 \) to 7.5 dB at \( M=32 \). This result is close to the \( \text{NF} \) prediction in the previous section. The \( 1/f \) corner was around 2MHz.
The current consumption without the negative conductance at 1 GHz LO is 18 mA (including 8 mA of clock circuitry (i.e. on-chip drivers and divider)), and 1.6 mA more for M=32. The clock divider frequency range (i.e. also the receiving RF frequency) is 0.2-2.6 GHz, where it consumes 2.8-19 mA. The maximum Gate-Source voltage of the mixer switches is equal to the 1.2V supply. The LO leakage to the RF port is less than -75 dBm. The optimum IIP3 has been measured for 5 samples. The optimum in-band IIP3 varies ±1 dB around +21 dBm and the corresponding M varies ±2 around M=32.

Table II benchmarks this work to other state-of-the-art receivers with high linearity and/or SFDR. Our front-end is more linear than [[3],[5]] where active RF blocks are present. Even compared to the mixer-first designs [[6],[7]] we achieve better in-band IIP3 while our SFDR in 1 MHz of 85 dB is the highest.

VII. CONCLUSIONS

Due to the strong relationship between linearity and voltage swing, it is challenging to improve linearity in advanced CMOS technologies with low supply voltages. Architectures with RF V-I conversion followed by a passive mixer and an OTA-RC Transimpedance Amplifier perform relatively well. In such architectures, the OpAmp can become the bottleneck, especially for wide channel bandwidth, where the amount of loop gain available for negative feedback is limited. Still high linearity is wanted, not only out-of-band but also in-band, as RF-filtering often is ineffective for close-in interferers. This paper shows how virtual ground imperfections due to OTA nonlinearity lead to distortion currents, which can be cancelled exploiting a negative conductance in parallel to the virtual ground node. Although the technique results in slightly degraded noise figure from 6 to 7.5 dB the in-band IIP3 (and IIP2) is improved by much more (>10 dB), resulting in-band SFDR=85 dB in 1 MHz bandwidth.

ACKNOWLEDGEMENTS

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APPENDIX

Appendix A

In this section, a 3\textsuperscript{rd} order Taylor approximation of $V_{\text{OUT}}$ versus $I_S$ (i.e. $V_{\text{OUT}}=V_{\text{OUT}}(I_S, I_S^3)$) of the transimpedance amplifier in Figure 9 will be derived. The following procedure will be applied:

1. $V_{\text{OUT}}$ is derived as a function of $V_{\text{VGND}}$, $V_{\text{VGND}}^3$ and $V_{\text{OUT}}^3$ \(\Rightarrow V_{\text{OUT}}=V_{\text{OUT}}(V_{\text{VGND}}, V_{\text{VGND}}^3, V_{\text{OUT}}^3)\).

2. The resulting relationship is rewritten as a function of $V_{\text{VGND}}$ and $V_{\text{VGND}}^3$, by using the definition of the 3\textsuperscript{rd} order Taylor coefficients \(\Rightarrow V_{\text{OUT}}=V_{\text{OUT}}(V_{\text{VGND}}, V_{\text{VGND}}^3)\).

3. The inverse function, $V_{\text{VGND}}$ as a function of $V_{\text{OUT}}$ and $V_{\text{OUT}}^3$, is written as a 3\textsuperscript{rd} order Taylor function by using the procedure explained in [15] \(\Rightarrow V_{\text{VGND}}=V_{\text{VGND}}(V_{\text{OUT}}, V_{\text{OUT}}^3)\).

4. $I_S$ is rewritten as a function of $V_{\text{VGND}}$ and $V_{\text{OUT}}$ \(\Rightarrow I_S=I_S(V_{\text{VGND}}, V_{\text{OUT}})\).

5. Substituting $V_{\text{VGND}}$ of step 3 in $I_S$ of step 4 makes $I_S$ to be a function of $V_{\text{OUT}}$ and $V_{\text{OUT}}^3$ \(\Rightarrow I_S=I_S(V_{\text{OUT}}, V_{\text{OUT}}^3)\).

6. Finally, by repeating the procedure explained in [15], the function of step 5 is inversed to obtain $V_O$ as a function of $I_S$ and $I_S^3$ \(\Rightarrow V_{\text{OUT}}=V_{\text{OUT}}(I_S, I_S^3)\).

Step 1 \(\Rightarrow V_{\text{OUT}}=V_{\text{OUT}}(V_{\text{VGND}}, V_{\text{VGND}}^3, V_{\text{OUT}}^3): We begin the derivation by expressing the feedback current $I_F$ at the VGND node and the OUT node (see Figure 9) as follows:

At VGND node: $I_F = \frac{V_{\text{VGND}}}{R_{F-\text{VGND}}} + G_{F-\text{VGND}} V_{\text{OUT}}$ \hspace{1cm} (14)
At OUT node: \( I_F = -\frac{V_{OUT}}{R_{F-OUT}} - G_{F-OUT} V_{GND} \) \hspace{1cm} (15)

Referring to the OpAmp nonlinear model, we equate the \( I_F \) in (1) to \( I_F \) in (15) as follows:

\[
\begin{align*}
\text{gm}_1 V_{GND} + \text{gm}_3 V_{GND}^3 + go_1 V_{OUT} + go_3 V_{OUT}^3 &= -\frac{V_{OUT}}{R_{F-OUT}} - G_{F-OUT} V_{OUT} \\
V_{OUT} &= -\left( \frac{\text{gm}_1 + G_{F-OUT}}{go_1 + \frac{1}{R_{F-OUT}}} \right) V_{GND} - \left( \frac{\text{gm}_3}{go_1 + \frac{1}{R_{F-OUT}}} \right) V_{GND}^3 - \left( \frac{go_3}{go_1 + \frac{1}{R_{F-OUT}}} \right) V_{OUT}^3 
\end{align*}
\]

Step 2 \( \Rightarrow V_{OUT} = V_{OUT}(V_{GND}, V_{GND}^3) \): \( V_{OUT} \) is defined as: \( V_{OUT} = \beta_1 V_{GND} + \beta_2 V_{GND}^2 + \beta_3 V_{GND}^3 \), which is a 3rd order Taylor approximation around \( V_{GND}=0 \), where \( \beta_1, \beta_2 \) and \( \beta_3 \) are the Taylor coefficients:

\[
\beta_{n=1,2,3} = \frac{1}{n!} \left( \frac{\partial^n V_{OUT}}{\partial V_{GND}^n} \right)_{V_{GND}=0}
\]

To derive \( \beta_1 \), we differentiate (16) with respect to \( V_{GND} \) as follows:

\[
\frac{\partial V_{OUT}}{\partial V_{GND}} = a + 3b V_{GND} + 3c V_{OUT}^2 \frac{\partial V_{OUT}}{\partial V_{GND}} \Rightarrow \frac{\partial V_{OUT}}{\partial V_{GND}} = a + 3b V_{GND}^2 \\
\therefore \beta_1 = \left( \frac{\partial V_{OUT}}{\partial V_{GND}} \right)_{V_{GND}=0} = a = -\left( \frac{\text{gm}_1 + G_{F-OUT}}{go_1 + \frac{1}{R_{F-OUT}}} \right)
\]

The same procedure is used to derive \( \beta_2 \) and \( \beta_3 \):

\[
\beta_2 = \frac{1}{2} \left( \frac{\partial^2 V_{OUT}}{\partial V_{GND}^2} \right)_{V_{GND}=0} = 0 \quad \text{and} \quad \beta_3 = \frac{1}{6} \left( \frac{\partial^3 V_{OUT}}{\partial V_{GND}^3} \right)_{V_{GND}=0} = b + a^3 c
\]
\[ V_{\text{OUT}} = \frac{a}{\beta_1} V_{\text{VGND}} + \left( b + a^3 c \right) V_{\text{VGND}}^3 \]  

(17)

Step 3 \( \Rightarrow \) \( V_{\text{VGND}} = V_{\text{VGND}} (V_{\text{OUT}}, V_{\text{OUT}}^3) \): We write the inverse of (17) in the Taylor series form: \( V_{\text{VGND}} = a_1 V_{\text{OUT}} + a_2 V_{\text{OUT}}^2 + a_3 V_{\text{OUT}}^3 \). Deriving \( a_1, a_2 \) and \( a_3 \) can be done by the procedure below.

First, let’s substitute (17) into its abovementioned inversed form as follows:

\[ V_{\text{VGND}} = a_1 \left( \beta_1 V_{\text{VGND}} + \beta_3 V_{\text{VGND}}^3 \right) + a_2 \left( \beta_1 V_{\text{VGND}} + \beta_3 V_{\text{VGND}}^3 \right)^2 + a_3 \left( \beta_1 V_{\text{VGND}} + \beta_3 V_{\text{VGND}}^3 \right)^3 \]

By equating the right to the left side of the equation above [15], the coefficients \( a_1, a_2 \) and \( a_3 \) are derived:

\[ V_{\text{VGND}} = \frac{1}{a} V_{\text{OUT}} - \frac{(b + a^3 c)}{a^4} V_{\text{OUT}}^3 \]  

(18)

Step 4 \( \Rightarrow \) \( I_S = I_S (V_{\text{VGND}}, V_{\text{OUT}}) \): Referring to \( I_S \) in Figure 9, we substitute the \( I_F \) (14) at the \( V_{\text{VGND}} \) node in the following equation:

\[ I_S = I_O + I_F = \left( \frac{1}{R_O} + \frac{1}{R_{F-\text{VGND}}} \right) V_{\text{VGND}} + G_{F-\text{VGND}} V_{\text{OUT}} \]  

(19)

Step 5 \( \Rightarrow \) \( I_S = I_S (V_{\text{OUT}}, V_{\text{OUT}}^3) \): By substituting (18) into (19), the following equation is obtained:

\[ I_S = \left[ \frac{1}{a} \left( \frac{1}{R_O} + \frac{1}{R_{F-\text{VGND}}} \right) + G_{F-\text{VGND}} \right] V_{\text{OUT}} - \frac{(b + a^3 c)}{a^4} \left( \frac{1}{R_O} + \frac{1}{R_{F-\text{VGND}}} \right) V_{\text{OUT}}^3 \]  

(20)

Step 6 \( \Rightarrow \) \( V_{\text{OUT}} = V_{\text{OUT}} (I_S, I_S^3) \): Finally, by inversing (20), we reach the following expression:

\[ V_{\text{OUT}} = \frac{1}{\left( \frac{1}{a} \left( \frac{1}{R_O} + \frac{1}{R_{F-\text{VGND}}} \right) + G_{F-\text{VGND}} \right)^3} I_S + \frac{\text{NL}_3 \left( \frac{1}{R_O} + \frac{1}{R_{F-\text{VGND}}} \right)}{\Omega_3} I_S^3 \]  

(21)
Where: $NL_3 = \frac{(b + a^2c)}{a^4}$ is related to the nonlinear terms of the OpAmp model.

**Appendix B**

In this section, the relation between $V_{\text{VGND}}$ and $I_S$ is derived to be used in the latch-up analysis section. In order to simplify this analysis, we assume a linear OpAmp (i.e. $g_{m3}=g_{o3}=0$). Consequently, (16) and (21) can be simplified as follows:

\[ V_{\text{VGND}} = \frac{1}{a} V_{\text{OUT}} \]  \hspace{1cm} (22)

\[ V_{\text{OUT}} = \Omega_1 I_S \]  \hspace{1cm} (23)

Combining (22) and (23), gives the following relation:

\[ V_{\text{VGND}} = \frac{\Omega_1}{a} I_S = \left[ \frac{1}{R_O} + \frac{1}{R_{F-\text{VGND}}} \right] + a G_{F-\text{VGND}} \]  \hspace{1cm} (24)

After that the negative conductance cancels the loading effect of $R_O$ on the VGND node, it injects current via $R_f$ that needs to be handled by the OpAmp output stage (see Figure 13 and Figure 17). Now if the negative conductance becomes too strong then the potential latch-up becomes a real risk. For the case of latch-up, (24) can be further elaborated to obtain the following equation:

\[ V_{\text{VGND}} = \left[ \frac{1}{R_{F-\text{VGND}}} - G_{\text{Latch-up}} \right] + a G_{F-\text{VGND}} \]  \hspace{1cm} (25)
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Figure 25: Measurements (a) S11 (b) Noise Figure, with LO=1GHz

Table I: IIP2 and IIP3 improvement

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<th>IIP3 [dBm]</th>
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<td>28</td>
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<td>32</td>
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Table II: Summary of measurement results and comparison to other state-of-the-art receivers

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[1] In-band BW is twice the zero-IF bandwidth around the LO frequency
[2] Includes the clock circuitry