DISTORTION COMPENSATOR

Inventor(s): SAKAMOTO KAZUMA; BRAM NAUTA + (SAKAMOTO KAZUMA, ; BRAM NAUTA)

Applicant(s): ASAHI KASEI DENSII KK + (ASAHI KASEI ELECTRONICS CO LTD)

Classification: - international: H03F1/32; H03F3/24
- cooperative: 

Application number: JP20110262188 20111130

Priority number(s): JP20110262188 20111130

Abstract of JP2013115725 (A)

PROBLEM TO BE SOLVED: To improve distortion compensation accuracy of a power amplifier. SOLUTION: An LMS algorithm using a feedback signal that is an output signal of a power amplifier input via an attenuator and pseudorandom data calculates a delay of an input signal to the power amplifier. A delay of an input signal to the power amplifier is adjusted on the basis of the calculated delay to match timing of the input signal to the power amplifier with a feedback signal including a fractional delay, and the delay-adjusted input signal where the timing is matched is used for distortion compensation of the input signal to the power amplifier to improve DPD mode distortion compensation accuracy. COPYRIGHT: (C)2013,JPO&INPIT;PROBLEM TO BE SOLVED: To improve distortion compensation accuracy of a power amplifier. SOLUTION: An LMS algorithm using a feedback signal that is an output signal of a power amplifier input via an attenuator and pseudorandom data calculates a delay of an input signal to the power amplifier. A delay of an input signal to the power amplifier is adjusted on the basis of the calculated delay to match timing of the input signal to the power amplifier with a feedback signal including a fractional delay, and the delay-adjusted input signal where the timing is matched is used for distortion compensation of the input signal to the power amplifier to improve DPD mode distortion compensation accuracy.