Interference Rejection at a Radio Receiver Input Exploiting Selective Feedback

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Abstract

The aim of this thesis is to study the feasibility of using feedback immediately at the antenna to improve the out-of-band linearity of receivers. The idea is to reject all signals at the antenna node, except for those in the wanted band, i.e. to effectively create a high-Q RF filter at the input of the receiver. An exception should be made for the desired signal which is available as a zero-IF baseband signal which is likely possible by upconverting it, breaking the feedback loop for the wanted signal. During the course time of the report, two architectures and a separate chapter for performance improvement techniques in terms of linearity are introduced. The main difference between the proposed architectures is the location of the gain stage. The first architecture has a feedback gain. Due to noise problem, the gain is moved to the forward path and the second architecture is formed. The resulting noise figure was found to be similar as in the case of a simple single stage common-base LNA. The linearity of the block itself also does not show a difference, but the interferers at the adjacent channels were attenuated at the input of the filter which brings more flexibility to the linearity constraints of the following building blocks of the receiver.
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1. Chapter 1: Introduction

In a zero-IF receiver architecture, the frequency band of interest is down-converted to low frequency range, low-pass filtered and processed. In other words, the desired band is frequency-translated using mixers. Since the band contains more than one communication channel, mixing of interferers at the adjacent channels may result in intermodulation products falling into the wanted channel which blocks the input signal. The purpose of this work is to eliminate out-of-band frequency components right at the antenna by using a negative feedback structure. This way, only in-band signals will pass to the mixer and contributions from other channels will be minimized.

First, expectations/ distinguishing aspects of these architectures will be explained. Their circuitry and simulation results regarding certain specifications will be displayed. Then, ideal components such as amplifier block will be replaced with appropriate transistor level circuits. These will be simulated, the results of which will be compared with hand calculations. Lastly, the obtained results will be evaluated, compared with targets and their usability will be discussed.

1.1. Motivation

Typical zero IF receiver architectures contain a band-pass filter (BPF) connected to the antenna such that the strong interferences at the adjacent bands can be eliminated before the LNA stage amplifies everything. After the amplification and down-conversion, the channel select filter passes only the channel of interest. This filter can be realized with two mixers which down-converts the frequency of interest (ωLO) to the DC level, and a low-pass filter.

![Figure-1: Conventional Receiver Architecture](image)

A BPF at the beginning can filter the adjacent frequency bands, but not the channels. At this point it is important to clarify that a frequency band can contain more than one
communication channel. The main purpose of this research is filtering also the adjacent channels to increase the sensitivity. This is not practical with an LC filter since its selectivity is limited by the quality of on-chip inductors. For example, in order to filter a channel with 20 MHz bandwidth (BW) and 1 GHz center frequency ($f_0$),

$$Q = \frac{f_0}{BW} = \frac{1 \text{ GHz}}{20 \text{ MHz}} = 50$$

is required which cannot be made on chip. Moreover, except some complex and costly ones, off-chip filters cannot be tuned over a significant frequency range. Therefore, filtering a channel at RF range has to be implemented in a different way.

Proposed is a feedback loop in which the channel of interest will be compared with the received signal and excess signal components will be subtracted from the received signal right after the antenna. The structure will be explained in more detail in chapters 2 and 3.

![Figure-2: Frequency Translated Feedback Loop Block Diagram](image)

Apart from expectation of increasing the out-of-band linearity, there are two main advantages of the above structure. First, since the subtraction of in-band signal components from entire frequency band implemented in Figure-2 before the mixers and LPF, BW requirements of these building blocks will be limited with the BW of the channel. So, differently from [1], wide-band operation will not be needed and this will relax the design of these blocks. Second, the center frequency of the filter is the LO frequency, which can be tuned to a desired value. Thus, $f_{LO}$ can be changed to select other channels.
1.2. Practical Goal of the Research

The goal is to improve the linearity for out-of-band interferers by 15 dB with respect to a conventional common base LNA. A bandwidth of 20 MHz and a center frequency of 1 GHz was chosen. The noise figure should be 6 dB or lower.

1.3. Single Stage Common-Base BJT LNA

It is important to compare a single stage common-base LNA with the modified one in terms of their noise and linearity performance. This way, a judgment on the usefulness of the circuits proposed in this work can be made.

\[ F = 1 + \frac{i_{n,Q}^2 \times \left( \frac{R_C}{A} - R_{eq} \right)^2}{V_{n,S}^2 \times \left( \frac{1}{1 + gmR_s} \right)^2} + \frac{V_{n,R}^2}{A^2} = 1 + \frac{\left( gmR_b + 0.5 \right) gm \times \left( \frac{R_C}{A} - R_{eq} \right)^2}{R_s \times \left( \frac{1}{1 + gmR_s} \right)^2} + \frac{R_C}{A^2} \]

Figure-3: Single Stage Common-Base BJT LNA
The circuitry simulated with $R_S = 50 \, \Omega$, $R_C = 500 \, \Omega$ and $I_b = 0.5 \, \text{mA}$. The simulated noise figure is $6.36 \, \text{dB}$.

### 1.3.2. Linearity

\[ V_{IIP3} = \frac{4}{3} \sqrt{3} V_T \approx 58 \, \text{mV} \approx -7 \, \text{dBm in 50} \, \Omega \]

In order to simulate IIP$_3$ point, a wanted (fundamental) signal and two interferers having an intermodulation product falling into that wanted frequency are used. Their magnitudes are kept the same and increased with the same amount. As the result, the magnitude level at which the IM$_3$ product of the interferes and the wanted signal intersect gives the IIP$_3$ point. It can be interpreted as the representation of the difference between the wanted signal and the blocking signals at the frequency of interest.

Desensitization point also measures the non-linearity. In that case, only the magnitude of an interferer which is placed onto an adjacent channel is increased. When it reaches a certain level, it starts decreasing the gain of the circuit. In contrast to IIP$_3$ point, desensitization point gives an idea about the behavior of the circuit in the presence of large interferes. This analysis relatively carries more importance for this research since the wanted signal can get weak through the long distance communication paths while the adjacent channels can get large signals from closer locations. This situation is represented via Figure-4.

![Figure-4: IM$_3$ Products of Interferers](image)

Simulation results show that the IIP$_3$ and desensitization points correspond to -12 dBm and -13.3 dBm respectively.
2. Chapter 2: Feedback Gain

2.1. System Level Design

2.1.1. Block Diagram

The intention is to suppress all frequencies except for the wanted channel by using feedback. For the wanted signal, the feedback loop should be inactive, so the signal can pass to the output without being attenuated. Feeding back the wanted signal with a loop gain (magnitude) of 15 dB gives out-of-band signal suppression of 15.6 dB. The block diagram of the proposed system level design is displayed in Figure-5.

From the block diagram, the relation between (matched) voltage (Thevenin) or current (Norton) from antenna, $U$, feedback that suppresses all signals out-of-band, $A$, terminated voltage or current at $R_X$ input and the transfer function of normalized translated filter, $H(s)$ is as follows:

$$U + X(1 - H(s))A = X$$
Solving for $X$ gives transfer function from $U$ to $X$ ($H_X$).

\[ H_X = \frac{X}{U} = \frac{1}{A(-1 + \frac{1}{A} + H(s))} \]

Multiplying with $H(s)$ gives transfer function from $U$ to $Y$ ($H_Y$).

\[ H_Y = \frac{Y}{U} = \frac{H(s)}{A(-1 + \frac{1}{A} + H(s))} \]

To summarize, during an in-band operation the filter will pass the signal to the output node ($H_Y = 1$) and there will be no attenuation from the source to the input ($H_X = 1$). On the other hand, an out-of-band signal will not be passed to the output ($H_Y = 0$) and the unwanted signal will be scaled down by the loop gain while going from the source to the input ($H_X = \frac{1}{1-A}$). The transfer function (TF) of the second order BPF, with center frequency $\omega_0$ and quality factor $Q$:

\[ H(s) = \frac{\omega_0}{Q} \frac{s}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \]

Substituting this TF in $H_X$ and $H_Y$ gives:

\[ H_X = -\frac{s^2 + \frac{\omega_0}{Q} + \omega_0^2}{(A-1)[s^2 - \frac{\omega_0}{(A-1)Q} s + \omega_0^2]} \]
\[ H_Y = -\frac{\omega_0}{(A-1)Q} \frac{s}{s^2 - \frac{\omega_0}{(A-1)Q} s + \omega_0^2} \]

So, overall the $Q$ is enhanced by a factor of "1-A" (Figure-8).
2.1.2. Schematic View

The schematic in Figure-6 has a signal source with 50 Ω resistance, a transconductance and a band-pass filter (BPF). As it is displayed in Figure-5 (b), the filter is composed of a down-converting mixer stage, a LPF and an up-converting mixer. The actual output will be taken from the end of LPF since at that point the in-band signal will be down-converted to DC level, filtered and made ready for further signal processing. In this case, there is also a need for an up-converted version of the signal since it has to be fed back to the input for the purpose of the out-of-band signal cancellation.

![Figure-6: System Level Schematic with Ideal Components](image)

2.1.3. Quality Factor and Center Frequency of the BPF

Center frequency of the filter, \( f_0 \), is the LO frequency which are given to the mixers as their second inputs.

\[
f_0 = 1 \text{ GHz}
\]

The bandwidth (BW) of the BPF is equal to twice the BW of the low pass filter (LPF). The required BW is 100 MHz. The transfer function of the LPF is given by:

\[
H(s) = \frac{1}{1 + j \frac{f}{f_c}}
\]
in which $f_c$ stands for the corner frequency.

$$f_c = \frac{1}{2\pi RC}$$

Since the BW is the double this value, a RC-time constant of 3.2 ns is used. Moreover, quality factor ($Q$) of 10 was accepted reasonable for the filter.

$$Q = \frac{f_c}{BW} = 10$$

2.1.4. Loop Gain

In order to find the loop gain, $|A|$, the circuit in Figure-7 is analyzed in terms of voltage. Furthermore, it is assumed that there is no current flow into node $X$ since it is looking to the base of a BJT transistor.

![Figure-7: Input Stage](image)

By inspection,

$$A = -g_m \times (R_s || R_m) = -\frac{1}{2} g_m R_s$$
It is known that the source resistance is equal to 50 Ω. Moreover, it is desired to attenuate out-band signals by 15 dB gain which corresponds to 5 V/V loop gain (magnitude). A will be set to -5 V/V which gives $H_x = \frac{1}{1-A} = \frac{1}{6} \frac{V}{V}$.

$$A = -\frac{g_m R_S}{2} = -5 \frac{V}{V}$$

$$g_m = 200 \text{ mS}$$

In Figure-8, the red plot represents the voltage level at the input and displays the signal attenuation of 15.6 dB while the blue plot represents the output of the BPF. Furthermore, the increase in the overall quality factor can be extracted from the same figure by inspection.
2.1.5. Noise Figure

In this part, the effect of noise at the input of the transconductor in the feedback path on the total noise power at the input of the whole system will be explored. For now, an ideal transconductor with a noise excess factor (NEF) defined as:

\[
NEF = \frac{V_n^2}{4kT \frac{1}{g_m}}
\]

will be used. This will give an estimate of the noise figure (NF) of the system when an actual transconductor (in transistor level, generating noise) is used.

\[R_S = R_m = 50 \, \Omega\]

Noise current coming from \(g_m\):

\[
i_{n,g_m}^2 = 4kT \times NEF \times g_m
\]

Noise current coming from source:

\[
i_{n,R_S}^2 = 4kT \times \frac{1}{R_S}
\]
Noise figure of the system:

\[
F = \frac{i_{n,R_s}^2 + i_{n,gm}^2}{i_{n,R_s}^2}
\]

\[
F = 1 + NEF \times g_m \times R_s + R_s
\]

With 50 \( \Omega \) source impedance, a transconductor with a NEF of 1 and a transconductance of 200 mS, this gives:

\[
NF = 10 \log(1 + 2 + 1) \approx 6.02 \, dB
\]

This was confirmed by simulation.

As it is seen above, 25 % of the noise contribution is coming from source while 50 % of it is coming from the transconductor. This shows that the noise factor has to be well below one, which means that more than one stage is needed since single stage transconductors are limited to NEF close to one [2].

2.2. Transistor Level Design

At this point, the BPF in the flow diagram will be treated as a switch for analytical purposes. The switch will be open during an in-band operation while it will be closed during an out-band operation. The circuit will be analyzed separately for in- and out-of-band inputs, with the switch closed when analyzing noise since this is important only in-band.

2.2.1. Schematic View

The circuit is composed of a differential pair and a common-base transistor. The working principle is based on setting the input impedance seen by the antenna either to 50 \( \Omega \) or to 5 \( \Omega \). When an in-band signal arrives, the BPF will pass the signal without applying an attenuation and the signals at the input nodes of the differential amplifier
will be equal. There will be no AC current passing through the differential pair. Consequently, there will be no small signal voltage drop between emitter and base terminals of $Q_0$ which will not draw any small signal current and will make the resistance seen when looking into its base high ohmic. As a result, the impedance seen by the antenna will be equal to the impedance seen when looking into the emitter of $Q_2$ which is equal to $\frac{1}{g_{m_2}}$. This value can easily be set to 50 Ω which is the main reason for choosing this common base architecture.

On the other hand, when an out-band signal arrives, the differential amplifier will start carrying small signal current. There will be a feedback loop built at the input which will decrease the input impedance to below 5 Ω. The matching will be destroyed and the signal level at the input will decrease by approximately 15.6 dB. The required component values such as bias current, resistor values will be calculated in the following section.

![Schematic](image)

**Figure-10: Schematic**

### 2.2.2. Input Impedance

DC operating point of $Q_2$ determine its transconductance which depends on the impedance matching constraint for the in-band operation.
Equivalent input resistance seen by the antenna during the out-of-band operation can be calculated as:

\[ R_{\text{in}} = \frac{1}{g_{m,2}} = 50 \, \Omega \]

\[ g_{m,2} = \frac{I_{C,2}}{V_T} = \frac{I_{C,2}}{25 \, mV} = 20 \, mS \]

\[ I_{C,2} = 0.5 \, mA \]

In order to provide 15.6 dB attenuation from the source to the input of the circuit, the loop gain \( A \) is set to 5 V/V.

\[ A = \frac{1}{2} g_{m,0} \frac{g_{m,2} R_S}{1 + g_{m,2} R_S} R_C = 5 \, V/V \]

\[ I_{C,0} \times R_C = 500 \, mV \]

The resistance \( R_C \) depends on the collector current \( I_{C,0} \) which is half of the tail current, \( I_1 \). At the end of next section the required quiescent current for a noise figure of 6 dB will be determined.

**2.2.3. Noise Figure**

Since the translated filter and the LNA are the first blocks of the receiver, their noise is directly added to the input, amplified and passed to next stages. This section will only take into account the contributions of the circuitry shown in Figure-10. The mixers, the filter and the bias sources will be assumed noise-free.

There are 5 main contributors to the noise figure, namely \( Q_0, Q_1, Q_2, R_0 \) and the source resistance which represents the antenna. It can be seen from the schematic view in
Figure-10 that $R_{C,t}$ is not part of the loop and therefore its effect can be neglected during the calculation. Moreover, since $Q_0$ and $Q_1$ transistors are identical, they will contribute the same amount noise. In the calculation, only one of them, $Q_0$, will be taken into account and this contribution will be multiplied by two.

In Figure-10, the noise contributions of these 5 elements are shown. First, the noise voltage at the collector of $Q_0$ ("NODE") generated by $Q_0$, $Q_1$ and $R_C$ is calculated. Then, this contribution is translated to the input node and added to the noise voltage generated by the source resistance ($R_S$) and $Q_2$.

![Diagram of noise generators](image)

**Figure-11: Noise Generators**

Input referred voltage noise generated by $Q_0$ or $Q_1$:

$$V_{n,Q_0}^2 = 4kT \left( g_{m,0} \times r_{b,0} + \frac{1}{2} \right) \times \frac{g_{m,0} \times R_C^2}{2} \times \left( \frac{g_{m,2} \times R_S}{1 + g_{m,2} \times R_S} \right)^2$$

Input referred voltage noise generated by $R_C$:

$$V_{n,R}^2 = 4kT \times R_C \times \left( \frac{g_{m,2} \times R_S}{1 + g_{m,2} \times R_S} \right)^2$$
Input referred voltage noise generated by $Q_2$:

$$V_{n,Q_2}^2 = 4kT \times \left( g_{m,2} \times r_{b,2} + \frac{1}{2} \right) g_{m,2} \times \left( \frac{R_S}{1 + g_{m,2} \times R_S} \right)^2$$

Input referred voltage noise generated by $R_S$:

$$V_{n,S}^2 = 4kT \times R_S \times \left( \frac{1}{1 + g_{m,2} \times R_S} \right)^2$$

Noise factor:

$$F = 1 + \left[ \left( g_{m,0} r_{b,0} + \frac{1}{2} \right) \times \frac{g_{m,0} R_C^2}{2} + R_C \right] \times g_{m,2}^2 R_S + \left( g_{m,2} r_{b,2} + \frac{1}{2} \right) g_{m,2} R_S \quad (Z)$$

It is known that:

$$g_{m,2} = \frac{1}{R_S} = 20 \text{ mS} \quad (X)$$

$$R_S = 50 \ \Omega$$

Furthermore, since $$A = \frac{g_{m,0}}{2} \times R_C = 5 \text{ V/V}, \ R_C$$ can be written in terms of $g_{m,0}$ such that,

$$R_C = \frac{20}{g_{m,0}} \quad (Y)$$
Substitution of \((X)\) and \((Y)\) into \((Z)\) simplifies the noise factor to:

\[
F \approx 1 + \frac{2A^2}{g_{m,0} \times R_S} \left( g_{m,0} \times r_{b,0} + \frac{1}{2} \right) + \frac{r_{b,2}}{R_S} + \frac{1}{2} \tag{F}
\]

Using this result the bias current \(I_2\) for a reasonable noise figure of 6 dB can be found.

Assuming the product \(g_m r_b\) is kept constant and has the same value for all transistors,

\[
r_b \times g_m = \text{Const} \approx 0.5
\]

\[
r_b \times \frac{20}{R_C} = \text{Const}
\]

\[
r_b = \frac{\text{Const} \times R_C}{20}
\]

Since \(I_{C,0} \gg I_{C,2}\), \(Q_0\) will be bigger and its base resistance will be lower.

Substituting \(g_{m,0} = \frac{1}{2} I_1 \div V_T\) in \((F)\) gives:

\[
F = 1 + \frac{2A^2}{\frac{I_1}{2} \div V_T \times R_S} \left( g_{m,0} r_{b,0} + \frac{1}{2} \right) + \frac{g_{m,2} r_{b,2}}{g_{m,2} R_S} + \frac{1}{2}
\]

Choosing \(g_m r_b = \frac{1}{2}\) and using \(A = 5, \frac{V_T}{R_S} = \frac{1}{2} mA\) and \(g_{m,2} R_S = 1\) gives:

\[
F = 2 + 200 \times \frac{\frac{1}{2} mA}{I_1}
\]
Solving $F = 4$ for $I_1$ gives:

$$I_1 = 50 \text{ mA}$$

which is not feasible.

To find the noise figure that can reasonably be achieved, the quiescent current is limited to 20 mA, which gives a noise figure of 11 dB.

The results show that the simulated noise figure at a quiescent current of 20 mA is 12.68 dB. Furthermore, noise contributions of different noise generators matches with the hand calculations.

### 2.3. Conclusions

The reason for this high noise figure is that the input referred noise of the amplifier in the feedback loop is amplified by the loop gain (see the factor $A^2$ in $(F)$) while the wanted signal does not undergo any amplification. To obtain a noise figure of 6 dB, a large power consumption of 125 mW is needed. This makes this architecture unattractive. Limiting the power consumption to a more moderate 50 mW gives a noise figure of 12.7 dB.

Noise figure, linearity and stability are the most critical parameters for this circuitry. If the circuit satisfies the specification for the noise figure, the linearity check will be made. To go back to the very beginning, the purpose of this research is to increase the linearity of the whole receiver by eliminating all the signal components falling out-of-band frequency range and avoiding the interference of the intermodulation products which can be produced at the adjacent channels. So, if the linearity does not improve, the circuit appears to be useless. For the comparison, a single stage common-base LNA and its linearity performance was displayed at the beginning of the report.

In the next architecture, the gain stage will be employed on the forward path which will amplify both noise and the wanted signal.
3. Chapter 3: Feedforward Gain

3.1. System Level Design

In the previous architecture, the input referred noise of the feedback loop was amplified with $A^2$ and added to the input of the receiver. On the other hand, the wanted input signal was not amplified. Therefore, the Signal-to-Noise-Ratio (SNR) decrease with $A^2$.

In this chapter, a new architecture will be employed. This new architecture carries the same purpose which is passing the in-band signals by having matching between antenna and the rest of the circuit, while attenuating all other signal components with out-band frequencies by destroying the matching. The main difference will be that this architecture will employ the gain stage on the forward path. This way, the wanted input signal will be amplified with the same amount of gain as noise. As a result, the SNR will not be degraded.

3.1.1. Block Diagram

![Figure-12: Architecture with Forward Path Gain, Block Diagram](image)

When an in-band signal arrives it will be amplified and conveyed to the node $V_X$. Since the BPF will pass it without applying any gain or attenuation, it will be subtracted from itself giving zero input to the transconductor. Thus, the feedback loop will be ineffective. In this situation the LNA provides matching to the antenna.

Oppositely, when an out-band signal arrives at the input, it will be amplified with gain $A$ but will not pass through the BPF. Therefore, the input voltage of the transconductor will not be zero anymore and the feedback loop will take part in the
operation. As in the case of the previous architecture, the input impedance and consequently the input voltage will fall down.

The amplified signal passes through the BPF which is exactly the same as used in the previous architecture (Figure-5(b)). The output signal of the BPF which does not contain out-band frequencies is subtracted from the input signal of the BPF which does contain out-band frequencies as well. For now, the subtraction is implemented via a Voltage Controlled Current Source (VCCS). So, if there is an out-band signal which forms a voltage difference between the input terminals of the transconductor, the transconductor starts drawing current and decreasing the input impedance by employing an additional small impedance in parallel with input impedance of the voltage amplifier.

\[ Z_{in} = \frac{R_m}{1 + A_{gm}R_m} \]

3.1.2. Schematic View

The schematic is built with ideal components in order to get an impression about the functionality and the noise performance of the architecture. For the noise performance, representative noise sources are used and the effect of generated noise at the input is observed.

The input impedance of the voltage amplifier has to be 50 Ω in order to provide matching during the in-band operation. This is modeled with a matching resistor, \( R_m \).
3.1.3. Loop Gain

The calculation of the loop gain is exactly the same as in Section (2.1.4). The only difference from the first architecture is that this time the forward path gain is 10 V/V which is easily implementable with a single stage CB LNA.

The out-of-band signal attenuation is maintained to be approximately 15.6 dB. Therefore, 5 Ω resistance is introduced in parallel to 50 Ω. If the resistance seen when it is looked into the output of the transconductor is called as \( R_t \), then the transconductance value can be found as:

\[
g_m = \frac{1}{\frac{1}{A \times R_t} - \frac{1}{10 \text{ V/V } \times 5 \text{ Ω}}} = 20 \text{ mS}
\]

This point is very important for a trade-off which will be encountered in the later sections. By separating gain stage from the feedback loop, the gain is realized to be independent from impedance introduced. Now, the same amount of input impedance can be provided with different gain levels. This point will be made more clear later on.

3.1.4. Noise Figure

![Figure-14: Noise Generators](image-url)
Contributions to the input referred current noise,

- Coming from the source resistance ($R_S$):

$$i_{n,R_S}^2 = 4kT \times \frac{1}{R_S}$$

- Coming from the input resistance of the LNA ($R_m$):

$$i_{n,R_m}^2 = 4kT \times \frac{1}{R_m}$$

- Coming from the transconductor:

$$i_{n,g_m}^2 = 4kT \times NEF \times g_m$$

So, the noise factor is exactly the same as the one calculated for the first architecture in Section (2.1.5).

$$F = 1 + \frac{R_S}{R_m} + g_m R_S \times NEF$$

When the input resistance of both the LNA and the transconductor is assumed to be 50 $\Omega$, the noise figure becomes 4.8 dB for NEF of 1.

The result was verified through simulation. Thus, it can be concluded that this architecture is usable w.r.t. noise.
3.2. Transistor Level Design

In order to go from system level design to transistor level design, the voltage amplifier (LNA) and the transconductor were replaced with sub-circuits composed of BJTs. First, the LNA was replaced with single stage common-base amplifier circuit since its input impedance can easily be set to 50 Ω. Second, the transconductor in the feedback path was replaced with a differential BJT pair which can be used to subtract two signals from each other and provide gain.

3.2.1. Schematic View

![Transistor Level Schematic](image)
3.2.2. Input Impedance

For in-band frequencies the BPF will have the same signal at its input and output terminals. Therefore, there will be no small signal current flowing into the differential. So the input impedance seen by the antenna becomes equal to the impedance seen when looking into the emitter of $Q_0$ which is $\frac{1}{g_{m,0}}$ which should be equal to $R_S = 50 \, \Omega$.

\[ I_{C,0} = g_{m,0} \times V_T \approx \frac{1}{50 \, \Omega} \times 25 \, mV = 0.5 \, mA \]

During the out-of-band operation, the BPF will not pass the signal. So, the amplified input voltage is applied to the differential pair which has a transconductance of $\frac{1}{2} g_{m,2}$. The small signal current will be flowing through $Q_2$ will be equal to:

\[ i_{C,2} = \frac{1}{2} g_{m,2} A V_{in} \]

The impedance seen when looking into the collector of $Q_2$ is:

\[ R_{in,2} = \frac{V_{in}}{i_{C,2}} = \frac{2}{g_{m,2} \times A} \]

$A$ and $R_{in,2}$ will be set to 10 V/V and 5 Ω respectively. As a result,

\[ g_{m,2} = 40 \, mS \]

From which, the second bias current of the circuit, $I_2$ can be found as follows:

\[ I_2 = 2I_{C,2} = 2g_mV_T = 2 \times 40 \, mS \times 25 \, mV = 2 \, mA \]
The LNA supplies 0.5 mA DC current from the power supply towards the input node and the transconductor will draw 1 mA from the input node to ground. The difference of 0.5 mA is provided to the input node via an additional bias current source.

3.2.3. Noise Figure

Figure-16 shows the main noise contributors.

Input referred current noise, coming from $Q_2$:

$$i_{n,Q_2}^2 = \left(1 - \frac{g_{m,2}}{g_{m,2} + g_{m,3}}\right)^2 \times i_{n,2}^2$$
\[ \frac{1}{4} \times 4kT \left( \frac{1}{2} + g_{m,2}r_{b,2} \right) g_{m,2} \]

coming from \( Q_3 \):

\[ i_{n,Q_3}^2 = \left( 1 - \frac{g_{m,3}}{g_{m,2} + g_{m,3}} \right)^2 \times i_{n,3}^2 \]
\[ = \frac{1}{4} \times 4kT \left( \frac{1}{2} + g_{m,3}r_{b,3} \right) g_{m,3} \]

coming from \( R_C \):

\[ i_{n,R_C}^2 = \left( \frac{1 + g_{m,0}R_S}{g_{m,0}R_S} \right)^2 \times i_{n,R}^2 \]
\[ = 4 \times 4kT \frac{1}{R_C} \]

coming from the source:

\[ i_{n,S}^2 = 4kT \frac{1}{R_S} \]

coming from \( Q_0 \):

\[ i_{n,Q_0}^2 = \left( 1 - \frac{g_{m,0}R_S}{1 + g_{m,0}R_S} \right)^2 \times i_{n,0}^2 \times \left( \frac{1 + g_{m,0}R_S}{g_{m,0}R_S} \right)^2 \]
\[ = 4kT \left( \frac{1}{2} + g_{m,0}r_{b,0} \right) g_{m,0} \]

From this point, the noise factor can be calculated.
The values indicated below are known:

\[ g_{m,0} = \frac{1}{50} S; g_{m,2} = \frac{1}{25} S; R_S = 50 \Omega; R_{eq} = 25 \Omega; A = \frac{R_C}{R_S} \text{ V/V; } \]

\[
F = \frac{i_{nS}^2 + i_{nQ_2}^2 + i_{nQ_3}^2 + i_{nQ_0}^2 + i_{nRC}^2}{i_{nS}^2}
= 1 + \left( \frac{1}{2} + g_{m,2}r_{b,2} \right) \times \frac{g_{m,2}R_S}{4} \\
+ \left( \frac{1}{2} + g_{m,3}r_{b,3} \right) \times \frac{g_{m,3}R_S}{4} \\
+ \left( \frac{1}{2} + g_{m,0}r_{b,0} \right) \times g_{m,0}R_S \\
+ \frac{4R_S}{R_C}
\]

From the simulation results, it is also known that:

\[ r_{b,2} = 31 \Omega \text{ and } r_{b,0} = 31 \Omega \]

In order to have LNA gain of 10 V/V, \( R_C \) is set to 500 \( \Omega \). The resulting noise figure is:

\[ 10 \log(4.26) = 6.3 \text{ dB} \]

Simulation results show that \( NF = 6.36 \text{ dB} \).

Note that \( R_C \) and \( A \) are connected to each other such that \( A = \frac{R_C}{R_S} = \frac{R_C}{50} \text{ V/V} \). From the equation above it can be understood that by scaling the transistors up or increasing the resistor value connected to the collector of the LNA, the noise performance can be improved more.
3.2.4. Linearity

Intermodulation products of out-of-band interferers can fall into the wanted channel and blocks the wanted signal. First, the fundamental signals will be calculated assuming they are attenuated by the BPF. Then, the IM$_3$ products generated by these will be added as external signals, which are passed by the BPF. From this, the IIP$_3$ is calculated.

![Diagram](image)

**Figure-17: 1$^{st}$ order Signal Operation**

The large-signal transfer functions of the amplifier and the transconductor are described by Taylor Series.

\[
V_{out} = \alpha_1 V_{in} + \alpha_2 V_{in}^2 + \alpha_3 V_{in}^3
\]

\[
V_\beta = \beta_1 V_{FB} + \beta_2 V_{FB}^2 + \beta_3 V_{FB}^3
\]
Large-signal transfer function of the loop is:

\[
(-\beta_1 V_{\text{out},1} + V_S)\alpha_1 = V_{\text{out},1}
\]

\[
\frac{V_{\text{out},1}}{V_S} = \frac{\alpha_1}{1 + \alpha_1 \beta_1}
\]

Moreover, from the previous sections, the forward path gain and the feedback path gain are known.

\[
\alpha_1 = g_{m,0} R_C
\]

\[
\beta_1 = \frac{1}{2} \frac{g_{m,2}}{2} \frac{R_S}{2}
\]

The transfer function of \( A \) for the signals that fall outside the wanted band is:

\[
V_{\text{out},1} = \alpha_1 V_{\text{in}} = \alpha_1 \frac{1}{1 + \alpha_1 \beta_1} V_S
\]

The \( \text{IM}_3 \) product generated by the LNA due to these out-of-band interferes will be proportional to \( V_S^3 \), such that,

\[
V_{\text{out},3} = \alpha_3 \left( \frac{V_S}{1 + \alpha_1 \beta_1} \right)^3 = \alpha_3 \left( \frac{1}{1 + \alpha_1 \beta_1} \right)^3 V_S^3
\]

The interferes are subtracted from the input via the feedback network \( \beta \). The first order transfer function of \( \beta \) is:

\[
V_{\beta,1} = \beta_1 V_{FB} = \beta_1 \frac{\alpha_1}{1 + \alpha_1 \beta_1} V_S
\]
The IM\(_3\) product at the output of the feedback will be proportional to \(V_S^3\), such that,

\[
V_{β,3} = β_3 \left(\frac{α_1}{1 + α_1β_1}\right)^3 V_S^3
\]

Figure-18: In-band Signal Operation with Externally Added Inter-Modulation Products

The wanted signal ends up at the output with a gain of \(α_1\), such that, at the output,

\[
V_{out} = α_1 V_S
\]

\[
V_{out} = α_1 V_S + \frac{α_3}{α_1} × α_1 × \left(\frac{V_S}{1 + α_1β_1}\right)^3 + \frac{β_3}{β_1} × β_1 × α_1 × α_1^3 × \left(\frac{V_S}{1 + α_1β_1}\right)^3
\]

- For a degenerated common-base BJT: \(\sqrt[3]{\frac{|α_3|}{α_1}} = 58\ mV\).
- The large-signal transfer of a differential pair is:
So,

\[ I_{C,2} = \frac{l_2}{2} + \frac{l_2}{4V_T} V_{FB} + \frac{l_2}{48V_T^3} V_{FB}^3 \]

Thus,

\[ \sqrt{\frac{4|\beta_1|}{3\beta_3}} = 4V_T = 100\,mV \]

To write down the output voltage once again,

\[ V_{out} = 10V_s + 3V_s^3 + 1002V_s^3 \]

\[ II_{P3} \cong 0.0815\,V_{rms} \]

\[ p = \frac{V_{rms}^2}{50} \]

\[ II_{P3} = 10\log(0.1327) = -8.77\,dBm \]

The feedback network dominates because although the input to the common-base BJT is attenuated by \( \frac{1}{1+\alpha_1\beta_1} = \frac{1}{6} \), the input to the differential pair is \( \frac{\alpha_1}{1+\alpha_1\beta_1} \) which is close to one, and thus not attenuated.
As it can be seen in Figure-19, the IIP3 point was found to be -12 dBm. It is an indication of the interference by the out-of-band signals having the same power level with the in-band signal. In the following chapter, big interferers and their effect will be put into consideration since it reflects the actual situation at the antenna.

During the simulations, 1.15 GHz and 1.3 GHz are used as the frequencies of two main interferes which produce an IM₃ product that fall on to 1 GHz.

![IIP3 Point](image)

Figure-19: Simulated IIP3 Point

### 3.3. Conclusions

The drawback of the first architecture was eliminated and the noise figure of the system was improved significantly. The simulated IIP₃ of -12 dBm shows that the small-signal linearity has not improved with respect to a simple single stage common-base LNA. However, this can be improved via using various linearization techniques. Some of them will be employed in the following chapter.
4. Chapter 4: Linearity Improvement Techniques

4.1. Degeneration

Since it is known that the differential pair is making the largest contribution to the non-linearity, linearization techniques are applied to it. The degeneration resistors are connected to the emitter terminals while the total transconductance is kept constant.

In order to obtain the same base-emitter voltage on $Q_2$, the amount of current drawn is doubled. The purpose is increasing the tolerance of the differential input terminals to higher level input signals.

-4 dBm simulated $I_{IP3}$ point and -11.9 dBm simulated desensitization point was obtained.
4.2. The Multiple-tanh Principle

BJTs show non-linear transconductance by nature. i.e. overall $gm$ value of differential pair start decreasing when the voltage difference between the input terminals varies from zero. The multiple-tanh principle relies on introducing two transconductance having offsets with opposite signs to the circuit [4]. Eventually the maximum transconductance will have the same value as before but this time it will maintain its value for a larger input voltage range.

In order to realize offset two non-symmetric differential pairs are connected in parallel as displayed in Figure-21.

![Figure 21: The Basic Multi-tanh Doublet](image)

Both stages have one transistor with a relatively larger emitter area than the other transistor. The ratio among the emitter areas, $A$, determine the shift at maximum $gm$ value. The input-output characteristic of the transconductor is shifted horizontally by:

$$V_{offset} = V_T \log(A)$$

A ratio of 4 which is known with exhibiting flat portion of $gm$ on top by experience gives 36 mV$_{pp}$ horizontal shift. It can be observed from the graph in Figure-22 that the overall characteristic, SUM, tends to be smoother for a wider range. The transfer function acts linear when input voltage takes value between -20 and +20 mV$_{pp}$. 

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Eventually, higher IIP$_3$ point is expected. However, although the transconductor shows linear behavior for small input voltage, it acts even more non-linear than before when high input voltages are applied. At that point, 5$^{th}$ order harmonics cancel third order harmonics and become the dominant IM$_3$ products. This highly non-linear behavior can be guessed when it is looked at the Figure-22. The edges of overall gm are sharper than the individual ones with offset.

Figure-23: Simulated IIP$_3$ Point of Multi-tanh Doublet
5. Conclusion

First of all, overall quality factor of the filter is enhanced by a factor of "1-A".

Secondly, when the gain stage takes place on the feedback path, the input referred noise of the system is amplified by square of the gain while the input signal maintains its initial level. This causes high noise figure.

Lastly, in case a single stage common-base LNA is used as the gain stage on the forward path, the nonlinearity of the circuit is dominated by the feedback path.

Simulation results of studied topologies/ methods are displayed in Table-1.

<table>
<thead>
<tr>
<th>Structure</th>
<th>Simulated Noise Figure</th>
<th>Simulated IIP$_3$ Point</th>
<th>Simulated Desensitization Point</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single Stage CB BJT</td>
<td>4.65 dB</td>
<td>−5.9 dBm</td>
<td>−21.45 dBm</td>
</tr>
<tr>
<td>Frequency Translated Feedback Loop</td>
<td>6.36 dB</td>
<td>−12 dBm</td>
<td>−13.3 dBm</td>
</tr>
<tr>
<td>Degenerated Differential Pair</td>
<td>6.17 dB</td>
<td>−4 dBm</td>
<td>−11.9 dBm</td>
</tr>
<tr>
<td>Employing Multiple-tanh Doublet</td>
<td>5.77 dB</td>
<td>NA</td>
<td>−13.66 dBm</td>
</tr>
</tbody>
</table>

Table-1: Comparison Between Different Structures

The noise figure requirement (6 dB) is almost satisfied by both 4 topologies/ methods above. The LNA with selective feedback loop employing degenerated differential pair on the feedback path seems the one which shows the best performance among all. While its simulated IIP$_3$ point has slight improvement, simulated desensitization point displayed a significant difference, namely, ~ 10 dB. This is due to the increase in bias current of the building block which contributes to the non-linearity most. This building block is the transconductor on the feedback path for the second case and it has 4 times larger bias current than the single stage CB BJT. If the same amount of bias current which will draw the non-linearity products are used, the simulated desensitization points will also be similar.

On the other hand, the interferers are reduced up to $\frac{1}{6}$ of their initial value which significantly relaxed linearity requirements of the following building blocks in order to obtain high sensitivity. Also, a further improvement on introduced building block’s linearity can be made by increasing the value of degeneration resistors which required higher bias current. In such case, upper boundaries for power consumption have to be determined.
References


