9.3 Active Feedback Receiver With Integrated Tunable RF Channel Selectivity, Distortion Cancelling, 48dB Stopband Rejection and >+12dBm Wideband IIP3, Occupying <0.06mm² in 65nm CMOS

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The impedance transformation property of passive mixers enables integrated high-Q channel selection at RF with a programmable center frequency through a clock [1, 2]. As such, this technique is suitable for addressing both linearity and flexibility requirements in wideband and cognitive radio applications. However, given the typically low resistance level at the RF side of the receiver chain, the RC product necessary for filtering results in large capacitors, and, consequently, large die area that does not scale with technology. In addition, filter rejection at the RF side is limited by the resistance of the switches of the passive mixer. Thus, large switches are typically needed for moderate rejection values (50Ω switches for 16dB rejection [2]), which translates to higher power consumption in the LO buffers. Furthermore, filtering prior to the LNA [1] or eliminating it altogether [3] improves linearity at the expense of noise and switching harmonics being injected directly at the antenna node. Conversely, an LNA first architecture offers an opposite trade-off. This work demonstrates a highly compact design of a direct conversion receiver with an active feedback frequency translation loop to perform channel selection at the LNA output while simultaneously cancelling its distortion.

Figure 9.3.1 (top) shows the proposed architecture. Signals at the antenna are down-converted and amplified. Along the feedback path, the desired signal BW, now centered at DC, is rejected using a HPF, while interferers are up-converted and fed back at the LNA output. With a high loop gain, node ‘A’ becomes a virtual ground for interferers beyond the corner frequency of the HPF, which effectively creates a channel select filter at node ‘A’. Since the feedback loop sinks current, filter rejection at the RF side is not limited by the resistance of the down-conversion mixer switches. As opposed to other feedback-based receivers [4, 5], the proposed architecture incorporates the receiver’s down-conversion path within the loop to provide an IF output instead of having a separate rejection loop after the LNA with an RF output that needs further down-conversion.

The channel bandwidth is now determined by the corner frequency of the HPF (\(f_{\text{HPF}}\)) divided by 1+\(T_{\text{O}}\), where \(T_{\text{O}}\) is the loop gain (Fig. 9.3.1-bottom). That is, for a given bandwidth, the capacitance needed for channel selection, and therefore die area, is reduced by the available loop gain. The loop bandwidth (\(f_{\text{BW}}\)) sets an upper limit on the frequency range of interferers that can be suppressed. Such a filtering loop is therefore suitable for implementation in a modern high-speed process and its performance is expected to improve with technology scaling.

To cancel LNA distortion, the V-to-I conversion circuits of the LNA and feedback amplifier are matched (Fig. 9.3.2). Under this condition, a down-converted inverted replica of input interferers is forced at the output via the feedback action, causing the feedback amplifier to perfectly sink the distortion currents sourced by the LNA. This arrangement has several advantages: (1) It performs large signal linearization, (2) it is based on feedback and matching transconductances, which makes it robust to process spread, (3) it cancels LNA distortion caused by out-of-channel interferers without placing the LNA inside the loop, thus avoiding injecting noise and mixer harmonics at the antenna, and eliminating one extra pole from the loop which results in higher loop BW for the same phase margin, and (4) non-linearity of the feedback path is not a limitation. Due to the frequency translation between the input and output nodes, this cancellation holds as long as the BW of the LNA transconductance is high compared to the loop BW plus LO.

Figure 9.3.3 shows the implemented receiver architecture, including an on-chip clock divider to generate the 4-phase LO necessary for differential I/Q operation. The entire design is based on self-biased inverters and switches, which offers a high Gain-Bandwidth product due to current reuse in inverters, eliminates the need for bias circuitry, and lends the design easy porting from one technology to another. All inverters are biased at roughly half the supply to maximize headroom and provide the same common mode level for cascading stages. The HPF is placed after the feedback amplifier to avoid its flicker noise from being up-converted to the channel band. For sake of simplicity to demonstrate the feedback loop, input matching is implemented with two 50Ω resistors to ground. The measurement interface provides isolation to measure the output without disturbing the loop. Noise and full channel bandwidth can be measured via the inverter buffers, while actual in-band gain and linearity can be measured via the large output resistors.

Figure 9.3.7 shows the micrograph of the chip implemented in standard 65nm Low Power (LP) CMOS. The chip is pad limited due to the multiple outputs required for testing, with an active area < 0.06mm² including the clock circuitry. Figure 9.3.4 (top) shows the measured RF-to-IF gain. The receiver achieves a gain of 30dB (measurement buffers de-embedded) with ±0.5dB variation for 1 to 2.5GHz LO, and a channel bandwidth of 5MHz (2.5MHz on either side of the LO). A stop-band rejection of 48dB is achieved at 250MHz offset. Figure 9.3.4 (bottom) shows a DSB NF in the range of 7.25 to 8.9dB for 1 to 2.5GHz LO, measured at a single differential output (I or Q). The increase in NF at lower LO is due to 1/f noise of the LNA which uses minimum-length transistors to achieve wideband input matching (measured S11 < -10dB from 1 to 2.7GHz). Figure 9.3.5 (top) shows the results of two-tone measurements. A wideband IIP3 > +12dBm for interferers at > 60MHz offset is achieved. The difference between in-channel IIP3 (about -20dBm) and wideband IIP3 indicates an improvement of > 33dB thanks to the feedback loop. Figure 9.3.5 (bottom) shows the blocker power level at which the small signal gain of the desired signal drops by 1dB (P-1dB). P-1dB exhibits a maximum of -3dBm for a blocker at 120MHz (>19dB improvement). The circuit core consumes 62mW (excluding clock circuitry and measurement buffers) from a 1.2V supply.

Figure 9.3.6 compares measured performance to other state-of-the-art receivers. The presented design occupies about 80 to 97% less die area, while achieving comparable or better performance. The bandwidth of 5MHz is suitable for most applications in the 1 to 2.5GHz range and increasing it would further reduce the die size. Compared to the highest stop-band rejection (50dB) reported by the superheterodyne architecture in [1], the direct conversion receiver presented in this paper achieves a comparable rejection of 48dB at about 5 times the frequency offset while occupying < 8% of the die area. Better or comparable wideband IIP3 of > +12dBm is measured at 2.5 to 13 times lower frequency offset (60MHz) compared to most reported values [4, 7]. Moreover, this design significantly outperforms previously reported feedback-based receivers [4, 5] in terms of gain, frequency range, stop-band rejection and wideband IIP3 while maintaining a comparable performance for other receiver parameters.

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References:
Figure 9.3.1: Proposed receiver architecture (top), and magnitude of impedance at LNA output ($Z_A$) versus frequency offset ($\omega - \omega_{LO}$), where $T_0$ is the loop gain (bottom).

Figure 9.3.2: Proposed LNA distortion canceling principle for out-of-channel interferers, where $g_{m3}$ is the third order transconductance nonlinearity.

Figure 9.3.3: Implemented architecture.

Figure 9.3.4: Measured RF-to-IF gain (top) (for negative frequency offsets, similar characteristics have been measured with ±0.1dB variation), and double-sideband noise figure (bottom).

Figure 9.3.5: Measured IIP3 (top), and blocker power level at which the small signal gain of the desired signal drops by 1dB ($P_{-1dB}$) (bottom).

Figure 9.3.6: Comparison to other state-of-the-art designs.