Design and Test of Micro-Electronic Fluidic Systems

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Abstract

The area of micro-electronic fluidic systems is rapidly developing into commercial products for many different applications. As a consequence, efficient testing of these systems becomes of key importance. This paper will show some of the results obtained previously and also discuss recent developments, which are considered to be important in testable design and testing of these systems.

1. Introduction

The area of micro-electronic fluidic systems has rapidly gained importance, as these systems can be used in many biological and pharmaceutical applications [1]. The potential features of these systems, like speed of operation, use of very small amounts of liquid, on-board detection, conditioning and vast signal processing, and their suitability for mass fabrication (disposable option) make them promising. However, testing these devices in a mass-production environment is still in its infancy and hampering their low cost on the market, although it is generally considered to be one of the main research test objectives in the next five years [2].

Except for an early paper [3], only recently [4-15] have papers appeared on this subject. Currently, the construction for testing these systems is rather cumbersome as figure 1 shows and unacceptable for mass-production.

In some applications, electronics is also merged with the fluidic modules, to perform control, signal conditioning and further data processing. Several applications, e.g. by HP are already on the market. Also for DNA determination, these devices have clear potential.

Additional problems with fluidic modules in the past, is that several modules contain moving static mechanical parts, which are relatively difficult to manufacture and almost impossible to test directly. An example of such a device, shown in figure 2, is a heating membrane-based fluidic pump.

![Figure 1: Example of the cumbersome set-up for testing micro-fluidic devices, including pumps and valves and hampering fast mass-production testing. The arrow indicates the MEF device.](image1)

The valves are very difficult to test, especially in the absence of a fluid. Several constructions have been suggested to reduce this problem [4], such as including a double metal layer for capacitive measurements (conversion of movement into a varying capacitance) or via a micro switch construction; however both implementations are far from trivial. However, it quickly became clear that fluidic systems without mechanical parts are much easier to test.

![Figure 2: A micro-fluidic pump with passive mechanical parts (valves). a) the cross-section, b) the actual implementation.](image2)
Recently, a new class of devices have emerged, containing no moving parts, and fully controllable by microelectronics. This device is referred to as a FlowFET, and is based on manipulating charges in a channel containing fluid by means of electrical fields. The required gate voltages are around 36V, but DMOS transistors being currently used in automotive CMOS chips can easily deliver these. Both these possibilities have stimulated the development of Micro-Electronic Fluid (MEF) Arrays. The development of the FlowFET [12] for the transport of fluid has had a positive influence on the testing of these devices.

The paper is organized as follows. In section 2, the construction, operation and transport capabilities of a fluid by the FlowFET will be briefly discussed along with the results of 3D simulations in the absence of defects. In section 3, an example will be given of a flow sensor, being an important device in many fluidic systems. For illustration, a defect (partial obstruction) will be assumed in the channel. It will be shown how a combination of physical understanding of the device operation and curve fitting results in an ECAD compatible fault model which can be used at higher levels, such as VHDL-AMS. In the final section, the (fault) modelling of fluidic devices at higher level is combined with established fault models in microelectronics to enable a joint fault simulation of an entire MEF array. In this way, e.g. the influence of faults in the fluidic part can be investigated on the entire system, thus enabling the development of test generation and design-for-test constructions.

2. The FlowFET and its Fault-Free Modelling

The original concept of the FlowFET was introduced in 1999 [18]. This has been the component used in the MEF array described in references [12-14]. Recently, an improved version has been designed, implemented and evaluated [17], which is the basis of the material in this section.

The basic structure is shown in figure 3. It is the result of thermal bonding of two parts (see dashed line). The basic material is Pyrex, and the gate electrodes consist of platinum. The electrodes are 175μm long, and 100μm apart. On top of the electrodes is a silica layer of 350nm. The implementation is seen at the bottom of figure 3. The length of the U-shaped channel is 19mm, with a bottom width of 30μm and a top width of 70μm. The depth of the channel is 18μm, and the fluid is an acetate buffer which fills the channel due to capillary forces. For more details, the reader is referred to [17].

![Figure 3: a) The cross-section of a FlowFET and b) an actual implementation.](image)

The voltage between the source (S) and drain (D) is 300V. The potential between the electrodes (G1, G2) and the fluid at the electrode location is 36 Volts. In figure 4, the predicted velocity distribution near the left and right side of the gate electrode are shown. The 3D simulations were performed using CDF-ACE+ [18] and employed 630k cells. As expected, the velocities near the middle of the channel under the electrode are the highest, while directly under the electrode the flow direction is reversed. Another interesting result is that the velocity vectors are equal in the channel before and after the electrode.

![Figure 4: Predicted velocity distribution (m/s) at the left and right side of the gate electrode from a full 3D simulation, using CDF-ACE+ [18].](image)

In figure 5, a slightly different representation is given that highlights problems associated with using a reduced channel length for the simulation (0.875 mm channel length). The velocity profiles away from the gate electrode are not fully developed indicating that a simulation of the entire 19mm channel must be performed.

Figure 6 presents the velocity distribution under the gate electrode, where the Zeta electrode potential is the changing parameter. As this potential is a function of the actual electrode voltage, it means that the flow can be completely controlled in two directions.

In order to verify the velocity simulations, a test setup is available including 0.9μ fluorescent beads in the fluidic channel. The current measurement problem is the depth dependency of the fluid velocity.
3. Fault-Modelling & Simulation of MEF Devices

The simulations for fault-free behaviour are the basis for fault simulations. As an example, figure 8 shows two cross-sections of a membrane-based flow sensor. It consists of a heater resistor Rh on a maze beam and sensor resistors upstream (Ru) and downstream (Rd).

A photograph of the moving fluid is shown in figure 7, with some particles (arrow) from which the velocity can be measured.

These results of fault-free devices give good confidence to move on to fault-simulations as the next step and to develop fault models for these devices.

Figure 8: a) Cross-sections and b) top view photograph of a micro-fluidic flow sensor with heating resistor Rh (2,5), and sensing resistors Rd (1,4) and Ru (3,6) on a membrane in the channel.

The fault-free simulation, in this case the temperature in the fluid, flow velocity 30mm/s, is shown in figure 9a. In the middle, the maze beam and resistors are located. Red denotes the highest temperature, while dark blue represents the lowest temperature. The sensors were used to verify the FEM simulations. In this particular device [7], seven different potential defects could be identified, based on experience as well as processing steps.

In figure 9b, the most disturbing fault, a large particle just before the beam has been simulated. One can observe the change in temperature distribution, and hence the resulting difference in functional behaviour of the flow sensor.

Figure 9: a) Simulation of the flow sensor temperatures at a specific power dissipation of Rh and a fluidic flow of 30mm/sec. b) simulation of the flow sensor temperatures at the same power dissipation of Rh and a flow of 30mm/sec in the case of an obstruction in the channel (white).
Based on the physical relationships, temperatures versus thermal resistances and capacitances, and simulation results for fault-free and faulty behaviour, models have resulted in an environment that is ECAD compatible. At the moment this is still a manual procedure, but it is planned to automate this process as already present in some commercial MEMS tools [20]. In our particular case, a SPICE model (figure 10a) has been developed for static evaluation. But also Matlab Simulink or VHDL-AMS models could have been derived. Figure 10b shows the FEM as well as SPICE simulated behaviour in the case of an obstruction (figure 9b).

The potential faults in a FlowFET have been evaluated based on the technological steps involved [3] and also experiences while testing devices [16]. Currently, three types of defects are anticipated. First, the thin oxide layer between the electrode and fluid can contain pin holes, resulting in a direct contact of the electrode with the fluid. This is a catastrophic fault. Second, because of the chemical mechanical polishing of the oxide, its thickness will not be everywhere the same. As a result, the Zeta potentials will differ from electrode to electrode. This causes parametric faults. Finally, the contacts from the source, drain and electrodes can be less low-resistive than desired. This also potentially yields in a parametric fault.

At these dimensions and implementation techniques, leakage and obstructive parts in the channel are unlikely to occur and cause faults.

However, the most recent developments with regard to fluidic channels include very shallow channels down to 50 nm [17]. In this case the physics and defects will be completely different from the previous discussed ones.

4. Fault-Simulation and Testing of MEF Arrays

Based on fault-free and faulty ECAD-compatible models of FlowFET, channel and flow sensor, it is now possible to construct a complete network or MEF array. An example of a chemical MEF array is shown in figure 11[12, 13], while in [21] a DNA MEF array is currently being investigated. By changing the relevant parameters in the models, the influence of particular defects on the entire behaviour (fluidic as well as electric) of the array is feasible. In our example here, we assume a jamming particle in a channel, hence changing parameter R1 (ellipse) in figure 10a.

Initially, Matlab Simulink was used for the simulations on the basis of availability of the software. Currently, ADVance MS™ of Mentor Graphics is being used.

Figure 12 shows the behaviour of the MEF in the case of a 73% blocking channel in figure 11 (indicated with X). The volume in the reaction chamber, being the vertical axis in figure 12, is measured indirectly by the flow sensors preceding the reaction chambers (figure 11).

In this example, the strength of being able to emulate defects in any MEF domain and subsequently simulate its consequences in terms of Design-for-Test structures and testing appears. As figure 12 reveals, by properly changing the addressing time of the FlowFETS, this defect can be detected at the output in combination with the flow-sensor data.
The current activities concentrate on using VHDL-AMS for the (fault) modelling of microelectronic fluidic devices, and extending the static simulations as carried out in figure 13 into dynamic ones.

Conclusions

The design and test of an advanced software controlled electronic-fluidic (MEF) microsystem has been discussed, as well as the testing strategy. The multi-domain microsystem is tested using different test strategies and DfT for different parts. The control and I/O electronics uses scan-based testing via conventional scan inputs and outputs. The high-voltage DMOS fluidic-electronic interface is tested subsequently by using an external Iddq monitor. The fluidics are tested by applying the electronic address mechanism and controlling the analogue high-voltage and address duration, as leakage and jamming particles in the channels are flow-velocity / volume dependent. The research marks a new step in non-mechanical electronic-fluidic testing, where electronics plays a major role in testing fluidics. Research is carried out to investigate the programming of the fluidic array via the TAP controller.

Currently, several projects have started within the PATENT-DfMM NOE framework in Europe, emphasizing on the (fault) modelling of fluidic systems, and overall high-level simulations of combined micro electro-fluidic systems. The first results show that innovative new testing methods can be applied to make these systems suitable for mass production.

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References


