PROCESS QUALIFICATION STRATEGY FOR ADVANCED EMBEDDED NON-VOLATILE MEMORY TECHNOLOGY ---- THE PHILIPS' 0.18μM EMBEDDED FLASH CASE

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ABSTRACT

A qualification strategy for advanced embedded non-volatile memory technology has been revealed. This strategy consists of: thorough understanding of the requirements, extensive use and frequent update of the FMEA (failure mode effect analysis), a qualification plan with excellent coverage of all the risk areas, implementing effective in-line and off-line measures and control, and check-off of all the tests with good results. With such a strategy in place, the Philips’ 0.18μm embedded flash technology has been successfully qualified for volume production.

INTRODUCTION

Advanced embedded non-volatile memory technology is one of the key technologies to realize system on chip (SOC) functionality. Such technologies require high performance, fast access, low voltage and low power operation non-volatile memories, together with advanced CMOS processes. Such a technology is often a very complex technology, making use of advanced STI isolation, multiple gate oxides, various well structures, advanced salicides, borderless contacts, high number of metal inter-connects, and low-K dielectrics in the backend [1]. The traditional standardized qualification programs based on product level life-tests and well known failure modes often do not provide enough coverage on possible new failure modes, and are lack of feed-back speed in case that new failure modes are encountered and results in enormous delay in final qualification. It is a great challenge to qualify such an advanced process in time with good coverage of all the possible failure modes, and to implement all the necessary and effective in-line and fast off-line measures to provide fast feed-back to the process development and to ensure the end-product reliability. In this paper, we will report and share our experience in the successful qualification of Philips’ 0.18μm embedded flash technology, that is, to our best knowledge, the first qualified embedded flash in 0.18μm CMOS process.

PROCESS QUALIFICATION STRATEGY

Figure 1 shows the general strategy used for a non-standard process qualification. The important elements are: (A) Have a clear translation of product requirements into device and process requirements. This is performed in the phase of project definition. (B) Perform an extensive process and product design FMEA (failure mode effect analysis). (C) Define a qualification work-plan that covers all the known possible failure modes. (D) Implement effective in-line and end-of-line detection methods, to provide continuous and fast feed-back to process development. These items (B to D) are frequently updated during the whole process development. (E) Carry out the qualification (check) work, compared to the process/product requirements. This is done in the qualification phase. (F) Implement improvement measures when needed, starting from updating the FMEA, and repeat the check till all requirements are met. When the previous steps (B to D) are done effectively, this iteration step F is often not needed. In the later sections, all these steps are explained with examples from the Philips’ 0.18μm embedded flash technology.

A well-defined qualification plan effectively covers all the possible failure modes appeared in FMEA. The first step is to translate the product requirements into device and process requirements. The results for Flash specific device part are the requirements for data retention (10 years), cell endurance (10,000 wear-erase cycles), related disturbs (program disturbs up to 1.3 seconds, and read disturbs up to 10 years), high voltage device lifetime requirements (the entire duration of programming and erasing time of the whole chip life time, 2,000,000 seconds) and worst case conditions (voltage and temperature). The results on the process part are: satisfy the high voltage requirements in the aggressive parts of salicide, borderless contacts, back-end process steps, and no impact of Flash process modules to the logic performance.

The second step is to perform product design and process design FMEA. The outcome of such brainstorm session is getting the high risk areas identified. In the Philips 0.18μm Flash FMEA, which has become a 29-page long document, the identified high risk items are: erratic bits, tunnel-oxide integrity, SILC, single bit retention failure, high-voltage device reliability, packaging reliability, irradiation immunity, endurance and retention fails. Table 1 lists the most important failure modes and actions/solutions to those.

A well-defined qualification plan effectively covers all the possible failure modes appeared in FMEA. For product level qualification in Philips’ 0.18μm Flash, two test-chips have been used to separately address the flash specific part (Flash test-chip: endurance, retention, all disturbs and high voltage part) and the logic, packing, and environmental part (logic test-chip: high temperature operation life, temperature cycling, pressure pot, etc.). The flash
specific tests should be performed on the whole of 16Mb test-chip, rather than on part of the chip. The wafer level device reliability assessments included all oxide/dielectrics integrity and stability tests, hot carrier tests, charging evaluation, ESD and latch-up characterization, electromigration and stress voiding tests, flash cell array evaluation and salicide reliability.

Table 1. The top three failure modes and defined actions.

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<th>Failure modes</th>
<th>Actions/solutions</th>
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<tr>
<td>Erratic bits</td>
<td>Design: 2T-FN-NOR array for erratic bits</td>
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<tr>
<td>Endurance</td>
<td>Design: 2T-FN-NOR employing uniform FN tunneling; Process control: isolation &amp; endurance tests at wafer release; Qualification: cycling the complete product</td>
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<tr>
<td>Single bit retention</td>
<td>Design: ECC; Process control: SILC measurements at wafer release; Qualification: gate stress after cycling.</td>
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<td>(incl. SILC induced)</td>
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The next step is to develop and implement effective in-line and off-line measurements. SILC has been recognized as one of the most important possible failure mode in advance flash technology [2]. A novel method has been implemented to get the SILC under control [3]. Such method including stressing a medium size flash array (4Mb) by bi-directional Fowler-Nordheim tunneling (to degrade the tunnel oxide), followed by a gate stress, and recording the lowest cell Vt value in the array (SILC characterization). Such a test has been implemented as an automatic test at wafer acceptance stage. Figure 2 shows such a trending of SILC parameter during process development. Huge number of data are collected on various experimental splits (tunnel oxide splits on growth-recipe and thickness). The experimental data in figure 2 are already very obvious without running the very time consuming flash life tests. The accelerated tests on product level shown in figure 3 are only an extra confirmation of data in figure 2.

The final qualification work becomes a kind of double-check-off (on wafer level and product level) of the reliability items with good coverage. Since the whole chip (16Mb) is cycled during endurance test to 10x the product spec, the possible weakest spot in the whole product can be detected: the control gate to bit-line isolation breakdown. This weakness in the deep sub-micron flash technology could become an endurance limiting factor when the alignment were not perfect or when irregularities are present (figure 4, left). Such weakness would have not been detected if less cycles or smaller memory parts were tested. Such weakness can be significantly improved by implementing a more smooth and rounded control-gate top corner (figure 4, right). With a quick iterations to update the FMEA, qualification plan update, process and in-line control improvements (more strict overlay control and a new release parameter at wafer acceptance on CG-BL isolation), the final qualification check yields excellent results, and the process is successfully qualified for volume production.

The strategy and methodologies used in the successful qualification of Philips' 0.18μm embedded flash technology have been briefly presented here. Important factors to guarantee good quality (and qualification) are: excellent understanding of the requirements, good coverage of FMEA, effective in-line and off line control with good coverage, and good coverage of the wafer level and product level qualification tests. Although the case of Philips' 0.18μm flash process is reported here, the philosophy of this qualification strategy applies to all qualifications of new processes.

REFERENCES