Strategies to Cope with Plasma Charging Damage in Design and Layout Phases

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Abstract—In this paper, strategies to cope with plasma charging damage in design and layout phases are discussed. A semi-empirical model is addressed first. With this model, a designer is able to predict the plasma charging induced yield loss of the circuit, if the antenna ratio (AR) distribution of the circuit is available. Then a novel first order self-balancing interconnect layout design is proposed to reduce the plasma charging damage. Moreover, the temperature effect on the protection diode is discussed and a strategic diode protection scheme for plasma charging damage is proposed. In addition to these general methods, a set of design rules is given to protect floating Metal-Insulator-Metal (MIM) capacitors from plasma charging damage.

I. INTRODUCTION

Plasma processes are widely used in the manufacturing of VLSI devices for etching and deposition. However, it also induces charging damage to the devices. Taking a metal-oxide-semiconductor (MOS) circuit as an example, a high electric field develops across the gate and substrate during plasma processing. It forces the charges through the metal lines and the underlying gate oxide and therefore degrades the gate oxide. Figure 1 illustrates this process.

![Figure 1: Schematic view of discharging paths](image)

In this equation, the failure fraction \( F \) is defined as the ratio between the failed antenna structures and the total test antenna structures. For MOS antenna structures, \( AR \) is defined here as the ratio between the area of exposed metal lines and the area of gate oxide.

II. USE OF DESIGN RULES

The antenna design rule is commonly used for sub-micron IC technology in semiconductor industry. It limits the maximum allowed antenna ratio (AR) for MOS transistors in the IC design and therefore limits the impact of plasma charging damage on the yield and reliability of products. Luchies et al. showed that smaller and fewer antennas can improve the yield in the presence of charging damage [1]. The design rules used in the industry depends on the company and technology. It ranges from zero to infinity. Zero means that every floating node in the circuit is tied down by protection diodes. Infinity means that no rule is established. In practice, the most common design rules fall between 100:1 to 1000:1 [2].

It is essential to set the maximum allowed antenna ratio. In production, charging damage is usually monitored by drop-in or scribe-line charging-damage test structures. Based on a serial antenna structures with varying AR from 1000 to 50000, a semi-empirical model is proposed to describe the relation between the AR\(_{MOS}\) and the plasma damage [3].

\[
\ln(1-F) = D(AR)^n. \tag{1}
\]

In this equation, the failure fraction \( F \) is defined as the ratio between the failed antenna structures and the total test antenna structures. For MOS antenna structures, \( AR \) is defined here as the ratio between the area of exposed metal lines and the area of gate oxide.
The constants of $D$ and $n$ could be get by fitting the measurement data from the antenna structures with different $AR$. $D$ is a constant that depends on the gate oxide thickness, the plasma process and the antenna material. $D$ and $n$ can be obtained by fitting the experimental results of charging testers with a series antenna structures. In the experiment discussed in this paper, $n \approx 0.46$ and $D \approx 0.001$.

Figure 2 shows that the model fits the measured data very well. The failure fraction at small $AR$ values that occurs more often in real circuits, can be extrapolated by using the proposed model. It is very useful for circuit designers. For instance, if $AR$ equals 100 in this developing process under study here, we predict a 0.9% failure fraction. This is sensibly high, indicating plasma charging problem in this process under development.

If the model could be verified by the experimental data from one's own process data, the failure fraction obtained on large $AR$ antenna test structures can be extrapolated to the failure fraction of smaller $AR$ structures. Therefore, the transistor plasma charging yield of the circuit can be calculated based on the $AR$ distribution of the circuit. Integrated circuit (IC) consists of a number of transistors with different $AR$. It will fail as soon as one transistor fails. We define here that the failed fraction of one transistor with antenna ratio $AR_i$ as $F_{AR_i}$, which can be calculated by Equation (1). The yield of one transistor is then $(1- F_{AR_i})$. Now the plasma charging affected yield ($Y$) of the whole IC can be calculated by using Equation (2).

$$Y = \prod_{k=1}^{p} \left(1 - F_{AR_i}\right),$$

where $p$ is total number of the transistors. Note that for this yield calculation, only the part of the transistor plasma charging effect is considered here. With this calculation, $AR$ design rule could be set more accurately to a specific layout of the circuit and the safety of away from plasma damage is ensured.

### III. Use of Diode Protection

Generally, a maximum allowed antenna ratio design rule is used to limit the plasma charging damage. Currently, computer-aided-design (CAD) tools cannot automatically layout the circuit with the antenna rule as one of the constraints. Antenna rule violation checking is done as a separate step after the layout is completed. When antenna rule violation is found, the common method of handling the problem is to insert a minimum size diode if space is available.

In 1989, Shone et al. proposed protection diodes as a means of avoiding wafer charging [8]. The diodes are connected in parallel to the gate providing an alternate leakage path for the plasma-induced current. Historically, the junction breakdown voltage has had a lower value than the gate oxide breakdown voltage and therefore, even a reverse bias has been effective in protecting gates. As the thickness of the gate oxide is scaling down, the gate oxide breakdown voltage strongly decreases. It was predicted that for oxides thinner than 11 nm, gated diode provides little or no protection [9]. However, later it was reported that the protection by diodes is still effective for 2.1 nm - 3.2 nm thin gate oxide FETs [10]. Even reverse diodes with high junction breakdown voltage can still offer some charging protection. This protection is due to their reverse bias leakage and can be adequate if they have a large enough area [11]. Apparently the protection diodes are more capable than what was anticipated. One of the explanations of the enhancement of the efficacy of the protection diode is
the presence of light. During the plasma process the diode reverse leakage current is enhanced by a photon generated current resulting from the light emission of the plasma [11]. However, the light effect is strongly affected by the metal on the top of the diode. If the diode is shielded from plasma illumination by metal, the reverse current of the diode rapidly decreases by more than one order of magnitude [12]. As the integration density of the VLSI technology continuously increases, the metal layers fabricated in the back-end processes increases from 3 layers to 5 layers, and even more. Furthermore, tilting of metal will block even more light, which makes it more likely that the protection diodes are shielded by the metal and there is no plasma-assisted photoconduction in these diodes.

In our study, the test structures are protected by different drain-well diodes. The schematic view of the different protection diodes is shown in Figure 4. The n+/p diode and p+/n diode are normal diode. However, the double-sided diode is floating n-well diode. The antennas of all test structures with protection at the antenna level are finger antennas with narrow spacing (0.32 μm). Since the leakage current of floating n-well protection diode (i.e. double-sided diode) is negligible at room temperature, it can be used for PMOSFET, NMOSFET and non-volatile memories (NVM) as well [12]. Considering the working potential of the MOSFET, n+/psub and p+/nwell, so called single diode can only be used for NMOSFET and PMOSFET respectively.

![Figure 4: Schematic overview of different protection schemes.](image)

The efficacy of different diodes has been compared by simulation and experiment. As presented in Table 1, the antenna structures protected by double-sided diode fail less than that protected by n+/p single diode.

**Table 1: Failed fraction (%) of NMOS transistor with protection diode at the antenna level.**

<table>
<thead>
<tr>
<th>Antenna</th>
<th>double-sided diode</th>
<th>n+/p diode</th>
</tr>
</thead>
<tbody>
<tr>
<td>Poly-Si</td>
<td>0.20</td>
<td>11.60</td>
</tr>
<tr>
<td>LIL</td>
<td>2.45</td>
<td>10.98</td>
</tr>
<tr>
<td>M2</td>
<td>0.25</td>
<td>2.45</td>
</tr>
</tbody>
</table>

LIL: Local interconnect level.

Double-sided diode: p+/nwell/psub

The leakage current of different drain-well diodes for plasma-charging protection has been simulated at high temperature [14]. The leakage current of the double-sided diode is enormously influenced by the temperature, as shown in Figure 5. By increasing the temperature by 100 degrees, the leakage current is about 1000 times higher.

![Figure 5: The leakage current of the double-sided diode is evaluated by high temperature. Note that the current values presented in the figure are absolute values. The bias voltage is ±0.75 V.](image)

The IV characteristic of different diodes under both positive charge and negative charge conditions are compared by simulation. The results are presented in Figure 6 and Figure 7.

![Figure 6: Simulations of the single diode and double-sided diode current at 400 ℃ under positive bias.](image)

![Figure 7: Simulations of the single diode and double-sided diode current at 400 ℃ under negative bias.](image)
efficacy of both single and double diodes in protecting very thin gate oxides. The double-sided diode shows better efficacy in the case that the gate of the MOSFET is positively charging. The leakage current of double-sided diode is 100 times higher than that of reverse biased n+/p single diode. Under negative charging, the n+/p single diode has higher current because it is forward biased. However, the leakage current of double-sided diode is still pretty high.

Considering the fact that one could not predict the charging priority of the plasma processes in advance, the double-sided diode is recommended. Especially for plasma charging damage induced by plasma-process, there were found during plasma deposition process at high temperature. However, diodes do represent additional circuit elements that need to be included in the circuit model. The additional load may degrade the circuit performance. The best strategy to identify and eliminate or at least minimize plasma charging damage is to fix process tools or parameters first. And then use design rules to limit the impact of the residual charging damage. When no other solutions are appropriate, then the use of protection diodes is recommended.

IV. Novel Self-balancing Interconnect Layout Design

The interconnect layout has a considerable effect on the charging damage induced by plasma-process, since it affects the current-density stress levels experienced by dielectric layers. It was reported that dense interconnect lines collect positive charges due to the electron shading (FS) effect [15] but sparse interconnect lines collect negative charges due to the extended electron shading effect (EES) [16]. In this section, a novel first order self-balancing interconnect layout design is proposed to reduce plasma charging damage in design phase.

In this study, two conventional finger-shaped antennas and one new dense-sparse interlaced antenna were designed. The dense-line antenna and sparse-line antenna arc commonly used in the study of plasma charging damage. In this experiment, they were designed with interspacing of 0.6 \( \mu \text{m} \) and of 5 \( \mu \text{m} \) respectively. The new dense-sparse interlaced antenna was designed as such that the spacing between the metal lines is alternately wide (5 \( \mu \text{m} \)) and narrow (0.6 \( \mu \text{m} \)). The schematic view of these structures is shown in Figure 8. The antenna ratios of these charging testers are 10000 and 100000. The antennas are all in metal 2 level.

Furthermore, a special structure combining 3 antennas with 3 transistors is designed as a special case study. The schematic view is shown in Figure 9 (a). Since they have 3 antennas and 3 transistors, they were called “TriMOS” structures. One transistor is in the middle (“TriMOS-M”), one is on the left (“TriMOS-L”), and another is on the right (“TriMOS-R”). The antenna ratio for each transistor of this “TriMOS” structure is 10000. Other two structures are also designed with minor modification based on this “TriMOS-L/M/R” structure. Because their antennas are so similar to the above “TriMOS” structure, we still give them a name with “TriMOS-” though these two structures do not have 3 transistors anymore. The one with two floating antennas is called “TriMOS-floating”, the other with two grounded antennas is called “TriMOS-ground”. Note that the floating antennas and grounded antennas are not connected to the MOS structure. Therefore, the antenna ratio for these two modified “TriMOS” structures is still 10000, the same with “TriMOS-L/M/R” structures. Note that the antennas are all in the same level (Metal 2 level). The schematic view of these structures is shown Figure 9. For some antenna structures, protection diodes are connected the gate at metal 3, in order to protect the gate oxide from damage produced by plasma process steps following the metal 2 step. For other antenna structures, protection diodes are not used. Therefore, we can verify the function of the protection diode. Additionally, if we want to measure \( Q_{bd} \) or \( E_{bd} \) of those antenna structures, we can stress them at high voltage, which is above the diode junction breakdown. Due to the limit of space, only NMOS transistors are used as test vehicle. However, we believe that, for PMOS transistor the result and mechanism we discussed in the following sections should be similar. Therefore, in the pictures and the context of the flowing sections, NMOS is not particularly mentioned.

![Figure 8: Schematic view of structure (a) conventional dense-line antenna structure with interspacing of 0.6 \( \mu \text{m} \), (b) conventional sparse-line antenna structure with interspacing of 5 \( \mu \text{m} \), (c) our new dense-sparse interlaced antenna structure with interspacing of 0.6/5 \( \mu \text{m} \).](image-url)
Figure 9: Schematic view of (a) "TriMOS-L/M/R" structure (b) modified "TriMOS" structure with two floating antennas (c) modified "TriMOS" structure with two grounded antennas. Note that the antennas are all in the same level (Metal 2 level).

As discussed in [17], the electrons and ions have significant difference in incident angular distributions. As a result of geometric and electrical shading, ions are so directional that none will hit the sidewalls on their way to the bottom. Electrons are so isotropic that most will hit the sidewalls and will stick there.

The imbalance between ions and electrons determines the amount of plasma-induced damage. How well they balance is related to the pattern of the antenna fingers (dense or sparse) and the phase of etching (during etching or over etching). The schematic view of dense antenna, sparse antenna, and "TriMOS-L/M/R" antenna structures during etching and during over etching are illustrated in Figure 12 and Figure 13 respectively. Since the antenna sketch of dense-sparse interlaced antenna structures, "TriMOS-floating" and "TriMOS-ground" structures are quite similar to the "TriMOS-L/M/R" structures, the interpretation for the reason that they failed less is same as that for the "TriMOS-L/M/R" structures, as illustrated in Figure 12(b) and Figure 13(b).

During etching, some sparse fingers collected negative charges and some dense fingers collect positive. The antenna of the "TriMOS-M" and "TriMOS-L/R" are still connected by the bottom thin metal layer. The collected ions and electrons may partly balance each other. Hence, the "TriMOS-M" and "TriMOS-L/R" are almost not charged, as shown in Figure 12(b).

During over-etching, the bottom layer is clear. The antenna of "TriMOS-M" and the antenna of "TriMOS-L/R" have been separated. The fingers of "TriMOS-M" are in the same situation as the "standard alone" dense finger structure mentioned above. It does not collect charges. Since the antenna of the "TriMOS-M" collects very little charge both during etching and during over-etching, the "TriMOS-M" suffers the smallest amount of plasma damage.

One side of the fingers of the "TriMOS-L/R" is in the same situation as dense finger structure. On one side the finger has narrow spacing, on the other side there is wide spacing. One side collects no charges and the other side collects a few negative charges, as shown in Figure 13(b).

However note that only one side of the antenna of left/right MOS collects negative charges, while both sides of the sparse antenna of the sparse antenna structures collect negative charges. The sparse antenna structures suffer more plasma damage than left/right MOS. The sparse antenna structures also suffer plasma damage during over-etching. This fact explains why the "TriMOS-L/R" fails less than the "standard alone" sparse antenna structures mentioned above. Hence, the "TriMOS-L/R" is negatively charged.

The failure fractions of normal MOS antenna structures and special "TriMOS" structures with same antenna ratio (AR = 10000) have been listed in Table 2. The failure fractions of MOS structures with new dense-sparse interlaced antenna failed much less than those with conventional dense antenna and sparse antenna, as shown in Figure 10. The conventional MOS charging structures both with 0.6 \mu m or 5 \mu m finger spacing, failed more than any of the "TriMOS" structures, as shown in Figure 11. For the structures either with diode protection or without diode protection, the middle antenna ("TriMOS-M") fails less than both the left antenna ("TriMOS-L") and right antenna ("TriMOS-R"). "TriMOS-floating" and "TriMOS-ground" structures are compared with "TriMOS-M", "TriMOS-L" and "TriMOS-R". Since they have almost the same antenna features, their failure fractions are quite close to "TriMOS-M" as what we expected. The failure fraction of these "TriMOS" structures is about 40 percent less than the dense or sparse antenna structures.

Figure 10: Comparison of the failure fraction of MOS with dense-sparse interlaced antenna, dense antenna, and sparse antenna.
This result indicates that the plasma-induced damage could be reduced if the interconnect lines are laid out like this way: one side of the line has narrow spacing but the other side of the line has wide spacing as the antenna in "TriMOS" structures or the dense-sparse interlaced antenna structure. Practically it might be difficult to apply this trick for the global IC circuits, but it is quite useful locally for specific transistors that are with quite high antenna ratios. By laying out the interconnect lines like "TriMOS-L/M/R" structures or simply adding dummy lines to the layout as in "TriMOS-floating" and "TriMOS-ground" structures, the risk and extent of plasma charging damage will be dramatically reduced.

**Figure 11:** Comparison of the failure fraction of normal antenna structures and "TriMOS-L/M/R" antenna structures.

**Table 2:** Failure fractions of normal MOS antenna structures and special "TriMOS" structures with same antenna ratio ($AR = 10000$).

<table>
<thead>
<tr>
<th>Failure fraction of antenna structures</th>
<th>0.6 µm spacing</th>
<th>0.6/5 µm spacing</th>
<th>5 µm spacing</th>
<th>TriMOS-L</th>
<th>TriMOS-M</th>
<th>TriMOS-R</th>
<th>TriMOS-floating</th>
<th>TriMOS-grounded</th>
</tr>
</thead>
<tbody>
<tr>
<td>With diode protection</td>
<td>6.7</td>
<td>NA</td>
<td>14.9</td>
<td>5.9</td>
<td>4.3</td>
<td>7.4</td>
<td>NA</td>
<td>NA</td>
</tr>
<tr>
<td>Without diode protection</td>
<td>58.2</td>
<td>27</td>
<td>61.3</td>
<td>19.9</td>
<td>16</td>
<td>20.3</td>
<td>18.7</td>
<td>14.8</td>
</tr>
</tbody>
</table>

NA: structures are not available.

**Figure 12:** Schematic view of the structures during etching.

**Figure 13:** Schematic view of the structures during over etching.
V DESIGN SOLUTIONS TO MINIMIZE PLASMA CHARGING DAMAGE FOR MIM CAPACITOR

In [18], results from plasma damage experiments on MIM capacitors are presented. The antenna effect is studied and modeled, and design solutions to minimize plasma damage are proposed.

Plasma charging damage to floating MIM capacitors is related to the size and shape of the antennas connected to both capacitor plates. The large area ratio of the interconnects that are connected to the two plates of the capacitor, leads to a potential difference across the insulator between the two plates. This unexpected potential difference stresses the dielectric of the floating MIM capacitor and causes the degradation of the device. We define here the interconnect lines connected to the top plate as top antenna, and the interconnect lines connected to bottom plate as bottom antenna. $AR_{T/B}$ is defined as the area ratio between top antenna and bottom antenna of the floating MIM capacitor.

As presented in Figure 14, the failure fraction is increasing with an increasing difference in top antenna and bottom antenna and falls to almost zero when the top antenna and bottom antenna are identical ($AR_{T/B}=1$). Therefore, in order to reduce plasma charging damage, the ratio between the areas of the interconnects connected to both plates of the floating MIM capacitor for each individual metal level should be close to unity.

As the bottom plate of some test structures is not connected to an antenna but to an extremely small pad, which is used for connecting to the up level. The effects of this very small bottom antenna (1.36 $\mu$m²) versus a large bottom antenna (10000 $\mu$m²) for a range of top antenna sizes are compared in Figure 15. For this extremely small bottom antenna, the failure fraction remains low and is independent of the top antenna sizes. This phenomenon is especially interesting because it opens the possibility for the introduction of metal bridges as a way of protecting the floating MIM capacitor. When the ratio of the two conductors connected to the plates of the floating MIM capacitor becomes too large, one of the antennas can be disconnected from the capacitor at the level of the antenna and reconnected again at a higher metal level by means of very small metal area. As such most plasma charging damage during the processing is avoided. Figure 16 shows a possible layout for the protection of the floating MIM capacitors by the use of a metal bridge.

![Figure 15: Effect on plasma charging damage of a very small antenna connected to one plate of the floating capacitor.](image)

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![Figure 14: $AR_{T/B}$ dependence on failure fraction for finger and plate antennas.](image)
VI. CONCLUSIONS

It is hard to avoid plasma charging damage during IC manufacturing. However, the plasma charging damage could be minimized by using tricks during design and layout phases.

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