A DC-coupled RF Amplifier in CMOS with DC-feedback

R. van der Werf, A.J. Annema, B. Nauta, A. Tudose *

MESA+ research institute, IC-Design group, University of Twente, P.O.Box 217, 7500AE, Enschede, The Netherlands.
Email: A.J.Annema@utwente.nl

* National Semiconductor B.V.
Bruistensingel 280, Den Bosch, The Netherlands

Abstract - A CMOS multistage RF amplifier with DC coupling is presented. A complete optimisation of the various stages is done to maximize the RF gain for a given power budget.

To decrease the effects of offsets and tolerances in high gain multistage amplifiers usually (lossy) AC coupling is used. The presented circuit employs DC coupling and DC control circuitry to avoid coupling-induced losses.

Compared to existing competing AC-coupled designs the presented one has much more gain at the same power consumption with a lower die area. For the 3-stage design vehicle, with Rsrec = 500Ω and Cout = 400fF, the maximal signal power gain at 4mA supply current is 33dB at 1.9GHz.

Keywords – High Frequency Amplifier Design, Mismatch and Drift Control, Active Common and Differential Feedback

I. INTRODUCTION

In RF transceivers high frequency signals have to be amplified. Taking into account the limited gain per amplifier-stage, fundamentally limited by e.g. the ratio between transistors fT and signal frequency, usually multiple cascaded stages are required to achieve the desired gain.

If DC-coupled, problems with multi-stage amplifiers arise due to mismatch, temperature drift, ageing and more: small offsets are amplified and accumulated. As a direct consequence an amplifier without any measures to ensure correct DC-biasing conditions is usually operated far outside its optimum operating range, which typically severely degrades its performance. The aim of this work is to optimize power gain for a given power budget, while ensuring correct operation in the presence of all kinds of quasi-DC disturbances. Suppression of offsets can be done by either using passive components or by employing active control circuitry. For fair comparison of the merits of the various methods, both AC and DC coupled RF amplifiers were optimized mathematically and in-circuit.

In the optimization, for a given set of conditions (source impedance, output load, signal frequency, National Semiconductor 0.25um CMOS process) it follows that a limited supply current can be optimally distributed among the amplifier-stages. For up to three-stage amplifiers this optimal current distribution can mathematically be derived.

By using optimized active DC voltage control the signal loss between stages is much lower than the loss in fully optimised AC-coupled 3 stage amplifiers, while the power consumption is only a fraction higher. In the optimum configuration each DC-coupled amplifier stage has its own merged differential/common voltage control loop. For the resulting offset-insensitive design, with Rsrec = 500Ω and Cout = 400fF, the maximal signal power gain of a three stage amplifier at 4mA supply current is 33dB at 1.9GHz.
II. DESIGN VEHICLE AT MAXIMUM GAIN

For this work, a 3 stage amplifier as shown in figure 1 was selected. The source impedance was assumed to be mainly resistive while the load was formed by the capacitive input of the next stage. Figure 1 also shows the initial circuit implementation.

**Voltage gain optimization**

In RF applications usually the power gain is relevant. For readability reasons we analyze voltage gain which can be easily translated into power gain for known source and load impedances. At RF frequencies the voltage gain of the circuit is:

\[
Av_{\text{total}} = Av_{\text{IN}} \cdot Av_1 \cdot Av_2 \cdot Av_3
\]

with

\[
Av_{\text{IN}} = \frac{1}{\sqrt{1 + \omega^2 \cdot C_{\text{in \_ stage}}^2 \cdot R_{\text{src}}^2}}
\]

\[
Av_{1,2} = \frac{gm_{\text{stage}}}{\omega \cdot (C_{\text{out \_ stage}} + C_{\text{in \_ next \_ stage}})}
\]

\[
Av_3 = \frac{gm_{\text{stage}}}{\omega \cdot (C_{\text{out \_ stage}} + C_{\text{out}})}
\]

Clearly the gain of each stage depends on its input transistors’ transconductance \(gm_{\text{stage}}\) and its combined output capacitance \(C_{\text{out \_ stage}}\) and its load impedance. Note that all these components are dependent on physical sizes and on bias conditions. In first instance it is assumed that the three stages are scaled copies of each other. Note that in that case the transistor gate-source overdrive voltages are the same for different stages. Defining now the scaling ratio between stages as:

\[
N_1 = \frac{C_{\text{in \_ stage}}^2}{C_{\text{in \_ stage}1}}, \quad N_2 = \frac{C_{\text{in \_ stage}}^3}{C_{\text{in \_ stage}2}}, \quad N_3 = \frac{C_{\text{out}}}{C_{\text{in \_ stage}3}}
\]

the partial voltage gain expressions become:

\[
Av_{\text{IN}} = \frac{1}{\sqrt{1 + \omega^2 \cdot \left(\frac{C_{\text{out}}}{N_1 N_2 N_3}\right)^2 \cdot R_{\text{src}}^2}}
\]

\[
Av_{1,2,3} = \frac{gm_{\text{stage}}}{\omega \cdot (C_{\text{out \_ stage}} + N_{\text{stage}} C_{\text{in \_ stage}})}
\]

With the assumption that the stages are scaled copies of each other a fixed (scale-invariant) ratio between transconductance and capacitances exists. Furthermore, noting that the effect of changing \(N_1\) is identical to changing \(N_2\) or \(N_3\), the function is symmetrical with respect to \(N\), it follows that the total gain equals:

\[
Av_{\text{total}} = \frac{1}{\sqrt{1 + \left(\frac{\omega R_{\text{src}} C_{\text{out}}}{N^3}\right)^2}} \left(\frac{gm_{\text{stage}}}{\omega \cdot (C_{\text{out \_ stage}} + N C_{\text{in \_ stage}})}\right)^3
\]

Straight forward analysis reveals that the optimum scaling ratio is:

\[
N_{\text{opt}} = \left(\sqrt{\frac{C_{\text{out \_ stage}}}{C_{\text{in \_ stage}}}} \cdot \frac{R_{\text{src}}}{1/ \omega \cdot C_{\text{out}}}\right)^2
\]

The optimal scaling ratio is rather independent from the bias settings of the amplifier stages. Using this optimal scaling ratio the maximal signal gain can be calculated. As shown in figure 2 the gain is a strong function of the amplifier’s bias settings. The optimum gate-source overdrive voltages can readily be calculated analytically.

**Figure 1:** A 3-stage RF amplifier as design vehicle

**Figure 2:** Maximum gain as a function of the gate-source overdrive voltage

Not only the maximum reachable voltage and power gain can be calculated, the required supply current follows as well. As first step it follows that:

\[
W_{\text{stage} \_ 3} = \frac{3}{2} \frac{C_{\text{out}}}{C_{\text{in \_ stage}3} L N_3}
\]

\[
= N_2 W_{\text{stage} \_ 2} = N_1 N_2 W_{\text{stage} \_ 1}
\]

with which it follows that:
\[ I_{\text{supply}} = \frac{3\mu C_{\text{out}}}{2L^2} \left( \frac{1}{N_3} + \frac{1}{N_3 N_2} + \frac{1}{N_3 N_2 N_1} \right) \]

would be the required supply current to get maximum gain. For our design vehicle this 65mA was well over the current budget. The next section presents gain maximalization under current budget restrictions.

Note that the previous derivation implies that spending more power than the optimum, indicated by the previous relation, not only is a waste of power but also results in lower performance.

**Voltage gain optimisation: with current budget**

In the previous section the optimisation was done for an unlimited supply current budget: the supply current followed from the gain maximalisation. One important property in that derivation was that we - independently- could select any \( N_1, N_2 \) or \( N_3 \). With the expression for \( I_{\text{supply}} \) in mind it is clear that this does not hold for a limited current budget, then for example \( N_1 \) follows from the combination of \( N_2 \) and \( N_3 \) and \( I_{\text{supply}} \):

\[
N_1 = \frac{1}{N_2 N_3} \frac{2L^2 I_{\text{supply}}}{3\mu C_{\text{out}} V_{\text{gs}}^2} - N_2 - 1
\]

A typical shape for the gain as a function of \( N_2 \) and \( N_3 \) and \( I_{\text{supply}} \) is shown in the next figure:

**III. Offset problems**

The transistors used in RF amplifiers are relatively small to get enough gain at the high RF frequencies. Because of their small sizes they exhibit relatively large spread; the input transistors’ threshold voltage spread appears to be dominant:

\[
\sigma_{\text{VT}} = \frac{A_{\mu}}{\sqrt{W \cdot L}}
\]

Other DC-type of disturbances include temperature drift \((\mu(T), V_{\text{th}}, T)\) and ageing. Considering that each stage has high DC-gain, all these effects cause quasi-DC voltage fluctuations for each of the amplifier-stages. The resulting large common voltage fluctuations per stage will severely disrupt the bias conditions of the amplifier; the effect of differential voltage fluctuation will be equally disrupting.

**IV. Offset solutions**

The typical solution to deal with offsets is using AC-coupling between stages. In that case input referred offsets of a certain stage propagate only through that stage. Disadvantages of AC coupling include the attenuation of the coupling, which can amount to 1.5dB best case, and the required chip area for the coupling capacitances.

To circumvent the losses associated with AC coupling, in this work DC coupling with active DC feedback was implemented. It appeared that the most efficient way to implement active DC control for both common mode and differential mode signals was using per-stage control steering at the PMOSTs’ gates (see figure 1).

**Figure 3: Maximum gain as a function of scaling ratios: power limited case**

The equation can be solved analytically, thereby directly yielding the maximum gain for a limited power budget. It should be noted that more complex calculations incorporating overlap capacitance's, the Miller effect and short channel effects will significantly increase the overall accuracy.

**Figure 4: Signal gain as a function of frequency: with and without DC control**
With these DC-control circuits, the low frequency signal gain of the circuit is suppressed significantly: in our design vehicle from roughly 2000 to 0.002 which makes the circuit very robust for any sensible amount of offset. The gain-frequency curves for the non-regulated and the controlled case (both without offsets) are shown in figure 4. At the same time the RF gain is also changed: this is mainly due to the additional load of the common and differential control circuitry. The 0.6dB signal loss for the current implementation is the result of the trade off between the accuracy (offset $\propto 1/$size) and the additional load capacitance ($\propto$ size) of the control circuitry. For the current implementation the gain decreases by approximately 0.6dB corresponding to an equivalent gain degradation of 0.2dB per stage.

V. Performance

In this section the performance of the design vehicle is presented. For comparison reasons the performance is compared to that of two other circuits. The first is a state-of-the-art AC coupled 3-stage RF amplifier; the second is a fully optimised (following the approach presented in this paper) AC coupled variant of the presented DC coupled circuit.

For benchmarking reasons, for all circuits the source and load impedances are the same, as are (about) the power consumptions and the signal frequency. The target of die-area for the DC coupled amplifier was the (best-case) die area of the fully optimised AC coupled 3-stage.

<table>
<thead>
<tr>
<th></th>
<th>this work</th>
<th>State-of-the-art</th>
<th>AC coupled optimized</th>
</tr>
</thead>
<tbody>
<tr>
<td>$P_{\text{supply}}$</td>
<td>10.8mW</td>
<td>11.8mW</td>
<td>10.4mW</td>
</tr>
<tr>
<td>$f_{\text{signal}}$</td>
<td>1.9GHz</td>
<td>1.9GHz</td>
<td>1.9GHz</td>
</tr>
<tr>
<td>Gain (power)</td>
<td>33dB</td>
<td>22.6dB</td>
<td>30.9dB</td>
</tr>
<tr>
<td>Area ($\mu m^2$)</td>
<td>2800</td>
<td>9210</td>
<td>2800</td>
</tr>
</tbody>
</table>

The needed chip area for the DC-coupled amplifier is mainly determined by the capacitors in the feedback-control-loop, whereas in the optimised AC-coupled amplifier the coupling capacitors between stages are dominant. The main advantage of the DC coupled amplifier is that there is no (significant) coupling induced gain degradation.

It clearly follows from the table that, firstly, fully optimising RF amplifiers with the method shown in this paper yields a significantly higher gain for the same power budget: both optimised amplifiers outperform the state-of-the-art implementation. Furthermore, the DC-coupled amplifier outperforms the optimised AC coupled version in (voltage- and power-) gain, for the same area, power and input signal.

VI. Conclusions

This paper presented a CMOS multistage RF amplifier with DC coupling, with complete optimisation of the various stages in order to maximize the RF gain for a given power budget. The DC coupled architecture was selected to circumvent losses induced by the common AC coupling of consecutive stages. To limit the effects of DC-type disturbances such as offset drift and ageing, per-stage feedback systems for differential and common levels were added.

Compared to existing competing AC-coupled designs the presented one has much more gain at the same power consumption with a lower die area. For the presented 3-stage design vehicle, with $R_{\text{src}} = 500\Omega$ and $C_{\text{out}} = 400fF$, the maximal signal power gain at 4mA supply current is 33dB at 1.9GHz. This achieved gain and power is a considerable improvement over other existing implementations, and over optimised AC coupled implementations.

VII. References