HIGH-VOLTAGE LEVEL TOLERANT TRANSISTOR CIRCUIT

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ABSTRACT

A high-voltage level tolerant transistor circuit, comprising a plurality of cascoded transistors, including a first transistor (T1) operatively connected to a high-voltage level node (3) and a second transistor (T2) operatively connected to a low-voltage level node (2). The first transistor (T1) connects to a biasing circuit (8), such as a voltage level shifter, providing a variable biasing level (V1) relative to a voltage level (V_{in}) at the high-voltage level node (3).

15 Claims, 9 Drawing Sheets