Fabrication of multi-layer substrates for high aspect ratio single crystalline microstructures

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Abstract

This paper reports a new method for making multi-layer substrates (MLS) for high aspect ratio single crystalline movable microstructures using a group of technologies, such as direct wafer bonding (DWB), chemical mechanical polishing (CMP), and reactive ion etching (RIE). As a first example, Si-SiO₂-polySi-SiO₂-Si sandwich wafers were fabricated using CMP and DWB. Subsequently, free-standing micro cantilever beams and double side clamped bridges were fabricated on these sandwich wafers using a one-run self-aligned RIE process, where polysilicon was used as the sacrificial layer. Polishing and bonding of low pressure chemical vapour deposition (LPCVD) polysilicon were studied. An LPCVD Si₃N₄ polishing stop layer technique was presented to accurately control the final thickness of the device layer. The uniformity of the device layer was improved as well. © 1998 Elsevier Science S.A. All rights reserved.

Keywords: Multilayer substrates; Silicon on insulator; Direct wafer bonding; Chemical mechanical polishing; Reactive ion etching; Microelectromechanical systems (MEMS)

1. Introduction

Up to date, the process incorporating direct wafer bonding (DWB) in making free-standing microstructures can be distinguished in two routes: (1) 'cavity' etching before bonding (e.g., Refs. [1–5]), and (2) sacrificial layer etching after bonding (e.g., Refs. [6–8]). The advantage of the first method is that the gap is defined by the etched depth of the cavity, which can be chosen freely, while in the second method, thickness of the sacrificial layer defines the gap depth. The drawback of the first method is, however, that at least two masks are necessary to make a micromechanical structure. On the other hand, fabricating microstructures from sandwich wafers (e.g., silicon on insulator (SOI) wafers) using the sacrificial layer etching technique enables self-aligned fabrication by using a one-mask process. In this technique, the structures are patterned and etched by reactive ion etching (RIE) on the top silicon layer of the SOI wafer, after which the structures are released by wet or dry isotropic etching.

When using the combination of DWB and RIE technologies in fabricating single crystalline silicon structures with high aspect ratio, the RIE lag was found to be a problem [5]. Furthermore, the thickness uniformity of the top silicon layer with a thickness of several tens of micrometers was not controllable, due to the lack of a stop layer. Such non-uniformity will cause problems during the release of the microstructures.

Previously, we have demonstrated a multi-step one-run self-aligned RIE process on commercial back etch silicon on insulator (BESOI) wafers [8]. The commercial BESOI wafers which were optimised for integrated circuits (IC) were not always found suitable for fabricating microstructures. We have also fabricated LPCVD polysilicon microstructures with limited aspect ratio on wafers having polySi-SiO₂-polySi-SiO₂-Si sandwich layers.

In this paper, a new method for making movable single crystalline micromechanical structures from multi-layer substrates (MLS) will be presented. Preliminary results of movable micromechanical single crystalline silicon structures that were made on the MLS will be demonstrated. A method for making uniform device layers using a chemical mechanical polishing (CMP) stopper technique will be discussed.

2. Multi-layer substrates for microstructures

We propose to fabricate movable microstructures from MLS (Fig. 1). The MLS consist of at least three layers: a device layer for making movable structures, a sacrificial layer for the air gap, and a substrate for the base of the devices, see Fig. 1a. Depending on the technologies that are used to fab-
Fabricate the structures, there may be additional intermediate layers between the device layer and the sacrificial layer, or between the substrate and the sacrificial layer. There are intermediate layers either function as an etch stopper or provide dielectric isolation. Then, movable micromechanical structures can be made on the multi-layer substrates by trench etching and sacrificial layer etching, see Fig. 1(b).

Fabrication of the MLS and the movable microstructures will make use of a group of technologies, such as DWB, CMP and RIE. Different materials, that cannot be integrated by other means, can be combined conjointly with the DWB technique. By providing extremely smooth surfaces, CMP will increase the freedom of direct bonding of materials having different surface qualities [9, 10].

Combining DWB and CMP, one has increased freedom in choosing the materials for the top device layer, sacrificial layer and the substrate. Single crystalline devices will be possible with improved mechanical and electrical properties. Furthermore, this process will be IC compatible if single crystalline silicon is used as the device material.

Unlike surface micromachining, where only devices having limited thickness are possible, with MLS high aspect ratio structures are possible, if recently developed cryogenic with high density source RIE techniques are applied [11].

3. Fabrication and results

3.1. Fabrication procedure for the Si-SiO$_2$-polySi-SiO$_2$-Si sandwich wafers

The process of fabricating the Si-SiO$_2$-polySi-SiO$_2$-Si sandwich wafers started with growing a thin (50 to 200 nm thick) thermal oxide layer on top of a 3 in., double side polished, (100) oriented silicon wafer, or 'seed' wafer. The oxide layer acts as an etch stop layer, due to the high etch selectivity of silicon to silicon dioxide in the RIE process. Then, a several micrometers thick LPCVD polysilicon layer was deposited on top of the oxidized wafer. A 1-h anneal at 1100°C in N$_2$ was conducted to release the stress inside the polysilicon layer. After CMP of the LPCVD polysilicon, the seed wafer was cleaned and fusion bonded to a 'handle' silicon wafer that was covered with a 1.5 nm thick thermal oxide layer. The bonded wafer pair was annealed for 2h at 1150°C. The seed wafer was thinned to the desired thickness by means of KOH etching followed by a brief CMP step. The fabrication process of the MLS is shown graphically in Fig. 2. A SEM photo showing the cross section of a MLS is presented in Fig. 3.

3.2. Polishing and bonding of LPCVD polysilicon

A CMP step is a must before the LPCVD polysilicon layer can be successfully bonded to a silicon wafer or an oxidised silicon wafer. The root mean square (RMS) roughness of the LPCVD polysilicon layer before CMP was measured to be between 5 and 15 nm, which is much higher than the 0.5 nm that is widely believed to be the critical RMS roughness of a
bondable surface. Furthermore, the polysilicon layer was covered with many protruding particles of several tens to 100 nm high (see Fig. 4).

Polishing and bonding of LPCVD polysilicon has been reported before, e.g., for micro accelerometers [12] and dielectric isolation applications [13,14]. However, there was no detailed description of the polishing and bonding process.

The CMP process was optimised for LPCVD polysilicon polishing with respect to the pads, the slurries and the process parameters such as the work pressure, pad temperature, the rotating speed, etc. The slurries and pads for final polishing of single crystalline silicon (SCS) wafers can be used to polish LPCVD polysilicon. However, the removal rate of LPCVD polysilicon was found to be more than five times higher than that of SCS (100), if the same process procedure is applied. We also found that the removed amount of LPCVD polysilicon does not have to be large. As soon as the protruding particles on the LPCVD polysilicon surface are removed, the CMP process should be stopped. Longer polishing will lead to the formation of pits on the polished LPCVD polysilicon surface. During CMP, the etch rate at the grain boundaries is often found to be higher than that of the grains. Also, polysilicon grains of different orientation are removed at different rates [15]. When final polishing slurry LS 10 and final polishing pad UR 100 were used, mirror-like polysilicon surfaces were achieved within 3 min CMP at a reasonable removal rate of about 30 nm/min. The surface topographies of the LPCVD polysilicon before and after CMP are shown in Fig. 4. The resulting RMS roughness of the polysilicon surface measured by atomic force microscopy (AFM) was typically 0.3 to 0.4 nm.

The room temperature bonding process was monitored with an infrared camera. After the first contact, an immediate bonding between the polished polysilicon layer and the oxidised wafer was observed. The propagating speed of the bond wave over the whole wafer was measured to be about 3 cm/min. Transmission electron microscopy (TEM) shows a well-bonded interface between polysilicon and silicon dioxide (Fig. 5).

The resulting room temperature bond strength of polysilicon bonded to silicon dioxide varied from 0.04 to 0.1 J/m², which is in the same range as that of silicon hydrophillic bonding. There is always a thin native silicon oxide layer on top of the polysilicon layer, just like that on a SCS surface. So, we believe that the bonding mechanism between the polysilicon layer and the silicon dioxide layer is the same as that between SCS to silicon dioxide.

3.3. Fabrication of the microstructures

After fabricating MLS, a high density RIE process [16] was used in etching and defining the structures. Then, several processes are possible to release the microstructures.

Here, the movable structures were fabricated in only one RIE run with four individual steps, see Ref. [8]. The fabrication sequence is shown in Fig. 6. Free-standing cantilever beams and clamped-clamped beams were made (Fig. 7a,b). In this case, the demonstrated structures were 25 μm high and the gap size was 1.6 μm. High aspect ratio SCS structures are only constrained by the RIE process, where etching of hundreds of micrometer deep structures is possible today [11,17].

No stiction was observed in the structures. This is one of the advantages of the dry releasing technique. No stress caused by the bonding interface was found. After the RIE process, there was no difference in etching behaviour between
the thickness and uniformity of the top device layer of several tens of micrometers thick.

The fabrication sequence for making MLS with an LPCVD Si$_{3+x}$N$_4$ polishing stop layer is shown in Fig. 8. First, narrow and deep trenches were etched using RIE and filled with LPCVD Si$_{3+x}$N$_4$ layer in the seed silicon wafer. The depth of these trenches defines the thickness of the device layer. The Si$_{3+x}$N$_4$ layer on top of the silicon wafer was removed using RIE. Then a thin thermal oxide layer and an LPCVD polysilicon layer were deposited. After brief CMP of the polysilicon, the seed wafer was fusion bonded to a handle silicon wafer that was covered with a thermal oxide layer. The seed wafer was thinned until the stop layer by wet etching and CMP. To date, we are able to achieve a less than 1 µm TTV of the top Si layer. A cross section of the trench filled with Si$_{3+x}$N$_4$ CMP stop layer is shown in Fig. 9.

In our preliminary experiment, the area of LPCVD Si$_{3+x}$N$_4$ CMP stopper layer covered only about 1% of the wafer. To achieve better and reproducible CMP stopper performance,
higher area ratio of LPCVD Si$_3$N$_4$ layer to SCS device layer is preferable. However, larger area of LPCVD Si$_3$N$_4$ layer may cause stress problem, which requires further investigations.

4. Conclusions

We have developed a new technique for making MLS that consists of Si–SiO$_2$–polysil–SiO$_2$–Si sandwich layers using CMP and DWB. Direct bonding between LPCVD polysilicon and silicon dioxide with good quality has been achieved after brief polishing of the polysilicon surface using the optimised CMP process. An LPCVD Si$_3$N$_4$ polishing stop layer technique has been developed to control the thickness and improve the uniformity of the top device layer. High aspect ratio SCS microstructures have been fabricated from MLS using the one run RIE process. This technology offers the following advantages: (1) SCS microstructures made from the MLS sandwich wafers offer good mechanical properties; (2) the thickness combinations of the top device layer and the sacrificial layer are freely selectable and high aspect ratio SCS microstructures are only constrained by the RIE process where etching of hundreds of micrometer deep structures is possible today; (3) no stiction was observed in the microstructures released on the sandwich wafers using the one run self-alignment process; (4) the thinner top oxide layer, used as a stop layer, facilitates the anisotropic RIE lag problem, while the thicker bottom oxide layer provides sufficient electrical isolation together with a smooth bottom; and (5) this technique is IC process compatible.

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References


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