Comb Capacitor Structures for Measurement of Post-processed Layers

D. Roy¹, J.H. Klootwijk², N.A.M. Verhaegh¹, H.H.A.J. Roosen², and R.A.M. Wolters¹

¹ NXP Semiconductors, Eindhoven, The Netherlands
² Philips Research, Eindhoven, The Netherlands

ABSTRACT

We present a simple comb capacitive measurement structure to monitor the properties of post-processed layers. These measurement structures are easily fabricated in a single step in the last metallization layer of a standard IC process, while the post-processed layer in this article is formed over these comb structures by spray coating. The capacitive coupling of the structure on the substrate is modeled based on the electric field distribution around the structure. The change in composition of this post-processed layer is analyzed in terms of measured capacitance values.

INTRODUCTION

To meet the increasing demands and performance requirements microelectronic industries have to deliver technological solutions that include smaller feature dimensions, introduction of new materials, and novel processing methods. Another approach is to increase the functionality of the existing chip by addition of extra integrated components for sensory applications like humidity sensors or gas detectors and other micro devices [1, 2]. Adding functionalities on top of metal layers of a finished chip is called post-processing. For sensing applications the change in properties of a post-processed layer (which may or may not be a CMOS based process) with the measured parameter needs to be sensed and converted into a measurable parameter. In this article comb capacitive test structures are used to detect the presence of such a post-processed layer and to study its properties. Comb structures are preferred since they have a large area exposed to the layer and can be processed in the same metal layer as the last metallization step of a chip. Comb structures also have a higher flexibility in tuning the capacitor value by changing the dimensions of the comb structures. These structures with different dimensions are fabricated on silicon substrates. Prior to the application of the post processed layer these structures are electrically modeled to study the different capacitors in the network. Then the post processed layer is applied on the structures and is electrically evaluated by capacitance measurements. In this particular study used a security coating as the post processed layer. This layer prevents physical attacks on an IC. Moreover, it provides the implementation of a physically uncloneable function (PUF) given the wide range of measured capacitance values.

TEST STRUCTURE

The test structures studied in this article are comb capacitor structures as shown in Fig.1 (a). These structures have two interlinked finger like metallic combs of equal height and width. Across the two combs a capacitance can be established, the variation of which is used in the analysis of the post-processed layer. The use of these test structures for the measurement meets the following requirements or advantages:

1. These structures are fabricated in one single metal layer.
2. The test structures are made in the last metal layer of the IC process and the post-processed layer is applied on top of the metal.
3. Optimizations of the capacitance for different post-processed layers are easily possible by varying length, width or distance between combs of the structure.
4. These structures have a significant amount of fringe capacitive coupling that increases the variation of the measured capacitance values with changes in the post-processed layer.

The test structures used for measurement of post-processed layers and the layer itself are fabricated on boron doped silicon substrates having a resistivity of 700–1300 ohm-cm. These comb structures are isolated from the silicon substrate by a 1.5 μm thick insulating layer of thermal oxide grown at 1100°C. On top of this oxide layer a 1μm thick aluminum layer is formed by sputtering and is patterned by lithography to form comb capacitive structures. The different post-processed layers are made from a liquid chemical matrix of aluminum-meta-phosphate (AMP) with inclusion of of TiO₂ (dielectric particles) and TiN (conducting particles) [3]. Over this patterned aluminum layer a 50nm SiO₂ passivation layer is formed by plasma enhanced chemical vapor deposition (PECVD) at 400°C to prevent chemical reaction between the post-processed layer and the metallic comb structures. This post processed layer is formed on top of the structures with an automatic spray coating unit. The layer is annealed at 400°C for 30 minutes in N₂ atmosphere. This makes it hard and porous and it binds the included particles in the porous matrix resulting in good adhesion to the substrate.
Figure 1: (a) Comb capacitor test structures; (b) parallel line approximated model for the comb structure on a Si substrate.

**ELECTRICAL MODELING OF TEST STRUCTURE**

The measured output from these test structure is a capacitance value. Detailed understanding of the measured capacitance involves determination of a capacitor model for these structures. This is done by capacitive measurements on the comb structures with different dimensions; width (w), length (l) and distance (d) between the combs. To simplify the capacitance calculations, interlinked comb structures are approximated to be two parallel lines as shown in figure 1(b). The height of the structures (h) is fixed to 1 µm. Test structures with four different lengths are available, \( l = 1000\mu m, 2000\mu m, 5000\mu m \) and 10000µm. For each of these different lengths there are structures with different width and distance between the combs. The possible widths of the combs are 2 µm, 5 µm and 10 µm and the possible distance between the plates are 1 µm, 1.5 µm, 2 µm, 2.5 µm, 3 µm and 5 µm.

Based on the field distribution between the combs and the silicon substrate, the capacitors established between the two combs structures are modeled as shown in Fig 2. The capacitors formed between the two combs are lateral capacitor (\( C_l \)) (\( C_{d1}, C_{d2} \) and \( C_{d3} \) are capacitors due to SiO\(_2\) passivation layer. The capacitance contribution due to this thin layer is neglected form the calculations) and lateral fringes (\( C_n, C_{d2} \)). For comb structures with parallel vertical edges, the lateral capacitance per unit length is estimated by a parallel plate approximation with \( d \) as distance between plates. The fringe capacitors arise due to concentration of charges at the corners of metallic structures. These fringe capacitances are a function of the width of the plates as well as the separation between the plates and its value dependence can be modeled as a polynomial of \( d^4 \). This fringe capacitance changes from zero to infinity as distance between the combs is varied form infinity to zero. For a fixed separation the charge density induced on each plate due to a finite potential on the other plate falls gradually with the increasing distance between each other. This gradually becomes insensitive to further increase on width. Another group of capacitors is the overlap capacitors (\( C_{o1}, C_{o2} \)) and overlap fringes (\( C_{n1}-\) \( C_{n6} \)) from the corners and the vertical faces of each comb to the silicon substrate. These capacitors can be seen as a MOS capacitor due to the stacking of metallic combs on silicon separated by an oxide layer. The overlap capacitance values cannot be calculated numerically since the substrate is not held at a fixed potential.

Figure 2: Capacitor model for comb structure on Si Substrate.

To model the capacitors in the network measurements were done by varying the width and distance between the combs for each structure for a fixed length. These capacitance measurements were carried out at 25°C with an HP4275A multi frequency LCR analyzer. The measured capacitance (\( C_l \)) includes overlap (\( C_o \)), lateral (\( C_l \)) and fringe capacitances (\( C_{fr}, C_{d2} \)). The capacitor \( C_{fr} \) is the combination of overlap capacitors \( C_{o1}, C_{o2} \). Overlap fringes \( C_{fr}-C_{n6} \) and the capacitance contribution due to the substrate. By comparing the capacitance network of the comb structure in Fig 2 to a parallel resistance- capacitance measurement network; the measured capacitance is approximated [5] to
\[ C_e = C_i + C_{f1} + C_{f2} + \frac{C_s}{2} \] (1)

The approximation used in deriving this equation is that all capacitors in the network are ideal and impedance offered by the substrate is zero. In this capacitor model presented, only the value of lateral capacitor is well established. To separate the contribution of different capacitors from the measured capacitance value, measurements are carried out by varying the distance between the combs and by changing width of the combs. In Fig 3(a) the capacitance is plotted with the reciprocal of distance (d) between the combs. As the distance between combs is large the lateral components \( C_i \), \( C_{fl} \) and \( C_{fr} \) becomes negligible and only the overlap component \( C_s \) remains. These can be obtained from the intercept of the curve with the capacitance axis. The value of \( C_s \) increases with the width of the combs due to an increase in the overlap capacitance values \( C_{o1} \) and \( C_{o2} \).

Similarly in Fig 3(b) the capacitance is plotted with the width of the combs and the curve is extrapolated to zero width. From the intercept the lateral component \( C_i \), part of \( C_{fl} \) and \( C_{fr} \) and the overlap component \( C_{o1} \) and \( C_{o2} \) including the substrate capacitances are estimated. If this intercept capacitance value in Fig. 3(b) is plotted with the inverse of the distance the lateral components can be eliminated and only the overlap components \( C_{fl} \) and \( C_{fr} \) including the substrate capacitance remains. By this analysis method all different capacitors in the network can be calculated. The application of a post-processed layer on the comb structures acts like a dielectric layer for the lateral capacitors of the network. The result is a change in the value of these lateral capacitors depending on the dielectric constant of the layer applied. This changes the measured value of capacitance making the comb structures ideal for measurement of a post-processed layer.

**Measurements**

The change in measured capacitance values with and without a post processed is shown in Fig 4. Capacitance values increase with a post-processed layer having an effective dielectric constant of 32. This increase is mainly due to the increased contribution of the lateral capacitance. The capacitance increase with increasing length of the combs is due to the increase in lateral area (increase in fringes is not that pronounced compared with increase in lateral value so the curve still remains linear).

Figure 3: (a) Capacitance with reciprocal of distance between the combs; (b) capacitance with width of the combs.

![Graph A](image1)

![Graph B](image2)

Figure 4: Capacitance with length of the structures.

The comb capacitance is not only sensitive to the variation in dielectric constant of the layer but also to the variation in the thickness of the post-processed layer. Figure 5 shows the variation in the capacitance values with thickness of the post-processed layer having a relative dielectric constant of 4 on top of the structures. The capacitance increases with thickness due to the increase in
the lateral fringe coupling, which saturates. Further increase in layer thickness has no effect on lateral fringes.

![Graph showing variation in comb capacitance with thickness of post-processed layer](image)

**Figure 5:** Variation in comb capacitance with thickness of post-processed layer.

The mechanism attributed to this increase in capacitance is first, the change in lateral coupling due to the presence of conducting TiN particles in the region between combbs. This can effectively be seen as a reduction in distance between combbs and there by increasing capacitance value.

![Graph showing capacitance values for different post-processed layers over the comb structures](image)

**Figure 6:** Capacitance values for different post-processed layers over the comb structures.

Fig 6 shows the plot of the measured capacitance value of a large number (600) of identical comb structures spread over a 6 inch silicon wafer for three different situations. The first case is comb capacitor measurements without a processed layer, while for the other two situations the structures have a homogeneous and a non-homogeneous post processed layer on top. The mixing of the uniform sized TiO$_2$ particles in an aluminum phosphate matrix results in a homogeneous precursor solution for the homogeneous layer. The addition of conducting TiN particles of varying size to this homogeneous precursor solution results in a non-homogeneous precursor solution. The size of TiO$_2$ particles is 300nm while the size of TiN particles varies from 500 nm to 3 μm. These precursor solutions are then spray coated and processed over the comb capacitive structures. The comb capacitance measurements without a post-processed layer show the lowest mean value of 36fF with a standard deviation of 5fF. The spread in capacitance value is due to the variation in the fabrication process and measurement accuracy. Application of a homogeneous layer with a relatively high dielectric constant of 32, results in a mean capacitance value of 212fF with a standard deviation of 43fF. This increase in mean capacitance value is due to the increase in lateral capacitance and fringes by a relatively higher dielectric constant layer over the comb structures, the overlap capacitance remains unaffected. The spread in capacitance value is also due to variation in the layer thickness due to the spray coating process. As shown in Fig 6 the non-homogeneous layers have higher capacitance values and a higher spread. The average capacitance value for this layer is 1125fF with a standard deviation of 405fF.

Fig 7(a) shows a SEM image of conducting particles in the dielectric layer. The presence of these conducting particles enhances the lateral capacitance value by forming a capacitive network between themselves and to the combbs as depicted in the SEM image. There is also an additional coupling between the conducting particles and the Si substrate. The resulting capacitive network with conducting particles in the vicinity of comb structures is schematically shown in Fig 7(b). Each of these conducting TiN particles creates an additional node in the equivalent capacitance network. The large standard deviation of the measured capacitance values can be understood from geometrical considerations. The size range of the TiN particles is 0.5-3 μm, the thickness of the coating is 3-5 μm and the distance between the metal combbs (d) of figure 1(b) is 1.5-2 μm for the measured structure (not in the SEM image). These TiN particles are incorporated in the dielectric layer in the lateral and vertical direction. This means that they will be distributed in position and size, leading to an unpredictable lateral and overlap coupling for each structure.
CONCLUSIONS

In summary comb structures are used as an effective tool to measure the presence of a post-processed layer and to study the properties of this layer. By varying the dimensions of this structure a model is described for the comb capacitors on silicon substrate. This model shows the different capacitive couplings through the post-processed layer, which significantly contributes to the measured capacitance values. Measurement of a security coating with these structures show that any change in the layer properties (e.g. dielectric constant and in-homogeneity) reveals itself as a significant difference in the measured capacitance values. The inclusion of conducting (TiN) particles in the layer modifies the capacitance network. This results in higher capacitance values due to the decrease in effective dielectric distance and in a wide capacitance distribution across the wafer due to local variation in the position and size of these TiN particles.

REFERENCE